A STUDY OF SOLID STATE
CIRCUITS FOR HIGH SPEED
DIGITAL COMPUTER APPLICATIONS

GEORGE A. FRIESE

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by

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ABSTRACT

This paper describes a study carried out by the writer as part of a preliminary evaluation of high speed digital circuitry to be used in a transistorized correlation computer. Three approaches to the problem of logical circuit design were considered: (1) the direct-coupled transistor, (2) the switching diode, and (3) the transistor-resistor. The circuits were effected using recent diffused base and drift type transistors and very fast switching semiconductor diodes.

A comparison of these systems was made on the basis of time required for a pulse to propagate through a one-bit full binary adder. Also considered were size of circuit packaging, power consumption, component value tolerance and supply voltage requirements for the three configurations. The study showed that the fastest pulse propagation was obtained with the direct-coupled transistor circuits, and that this type of system was preferable from nearly every other standpoint. The economical advantage gained in the switching diode and transistor-resistor circuits, however, must be carefully considered in computer applications requiring thousands of components. The transistor-resistor configuration was found to be very much slower than the other systems.

A byproduct of this work was a transistorized pulse generator with pulse repetition frequency variable from less than one mc to greater than 10 mc. Pulses with rise times of less than 30 mμ seconds and variable width were obtained.

The majority of the work described herein was conducted at the Firestone Engineering Laboratories, Monterey, California. The writer is duly grateful to this organization for the opportunity to conduct this study and wishes to express his appreciation to those who assisted him. Grateful acknowledgement is given also to Professor M. L. Cotton of the U. S. Naval Postgraduate School for his interest and suggestions.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

TABLE OF SYMBOLS

α, α_N	–Forward current transfer ratio, common base configuration
$f_{\alpha co}$	–Alpha cutoff frequency; the frequency at which the forward current transfer ratio is .707 of its low frequency value
ω_α	–$2\pi f_{\alpha co}$
i_C, I_C	–Collector current
i_E, I_E	–Emitter current
T_S	–Saturation delay time
T_{sw}	–Switching time
i_B, I_B	–Base current
I_{CS}	–Saturation collector current
V_{CE}	–Voltage, collector to emitter
V_{BE}	–Voltage, base to emitter
V_{CB}	–Voltage, collector to base
V_{cc}	–Voltage, collector supply
I_C (Max)	–Collector current, maximum rating
f_{sw}	–Switching frequency
T_p	–Propagation delay time; the time required for the output pulse to rise to 50% of its final value, using as a reference the time at which the input pulse attained 50% of its final value.
V_{bb}	–Voltage, base supply
x_N	–The logical input to the Nth X register
X_N	–The logical output of the Nth X register
$\overline{X}_N$	–The complement of the X_N output
β	–Forward current transfer ratio, common emitter configuration
T_r	–Rise time; the time required for a waveform to change from 10% to 90% of its final value.

1. Introduction

In the history of scientific achievements the transistor stands almost alone in the rapidity with which it has advanced from conception to a useful and refined state. Within a matter of a few short years, this device has reoriented nearly every major area in the field of electronics, the necessary research and production efforts rising to overcome inherent disadvantages with increasing success. While the transistor has brought many immediate improvements, the needs of the rapidly changing computer technology have continually presented new problems that must be solved. The trend toward replacing inefficient human decision-making and control with high speed computers has increased the amount of equipment that must be installed in aircraft, mobile systems for ground forces, guided missiles, and many other important applications, thus making size, weight, and power consumption extremely critical.

The early promise of the point contact transistor to solve the important problems presented by vacuum tube circuitry was jeopardized by poor noise figure and less than desirable stability characteristics. The advent of the junction transistor in the early 1950's showed that a solution to these problems was attainable and provided a wider range of power handling capacity. The upper frequency limit, however, was unacceptably low compared with the vacuum tube counterpart, and this, along with temperature limitations, became one of the last major developmental hurdles. By 1955, a big improvement had been obtained in the surface barrier transistor, which provides higher alpha cutoff frequency and is producible with good uniformity.

Today, as a result of continuing efforts to improve switching frequency capability, production of diffused base and drift transistors offers yet another order of magnitude of increase in the quest for high frequency operation. These devices provide alpha cutoff frequencies ranging up into the hundreds of megacycles and represent a tremendous stride toward the ultimate goal of high speed switching.

Along with the introduction and development of the transistor has come a wide variety of semiconductor diodes, among which is a type specifically designed for fast switching applications. These diodes, as in the case of the transistor, have steadily improved and presently are obtainable with recovery time as low as several mμ seconds.

1

In order to realize the benefits of new devices such as the transistors and diodes described above, a study of possible design techniques and their application to computer circuitry is valuable. Such a study is the subject of this work, its primary objectives being high speed switching and reduction in size of component packaging. Among other goals are the use of standard, available transistor types with no special selection for matching of characteristics; low power consumption; satisfactory operation with realistic fluctuations in supply voltages; and employment of resistors without preselection.

2. Circuit Considerations and Problems
    a. General Discussion
        The need for faster and more reliable circuits to improve
computer data handling capabilities has exerted a tremendous influence
upon design efforts. The incorporation of workable designs into a
current computer system, however, usually results in appreciable
delays, as the many problems of implementing such a system prevent
its immediate utilization. Consequently the computers presently in
use do not as yet have the benefit of the latest improvements in transis-
tor characteristics. As late as 1955 only a small number of experi-
mental transistor computers had been built and only within the last
year or so have relatively low speed, commercial computers been
available [1]. The diffused base and drift transistors now being
produced in large quantities will be able to increase switching speed
and also provide circuit simplification advantages.

        The digital computer, in general, consists of components
that perform the functions of information storage, logical "arithmetic",
counting, timing and control. The block diagram in Figure 2.1
represents, in general, the operations that are carried out in a typical
computer. The Arithmetic Unit requires some type of "temporary"
information storage device, or register, and an adder which performs
the logical switching operations. Transistors and diodes are ideally
suited for these purposes and it is the design of this portion of the com-
puter that will be considered.
    b. Design problems
        In operating the transistor as a high speed switch, which is
essentially the function it performs in most computer applications, its
inherent switching capability is of primary importance. It is this
characteristic that determines the extent of auxiliary circuitry needed
to obtain the desired switching speed. The most important parameter in
determining the transistor's high speed performance is its alpha cutoff
frequency, or $f_{\alpha co}$. This is the frequency at which α , the
forward current transfer ratio, is .707 of its low frequency value and is
related to the collector current response by the approximate expression
[2] :

$$ i_c(t) = \left(1 - e^{-\omega_\alpha t}\right) i_E \qquad (2\text{-}1) $$

where $\omega_\alpha = 2\pi f_{\alpha co}$ and i_E is a unit step function. From (2-1)
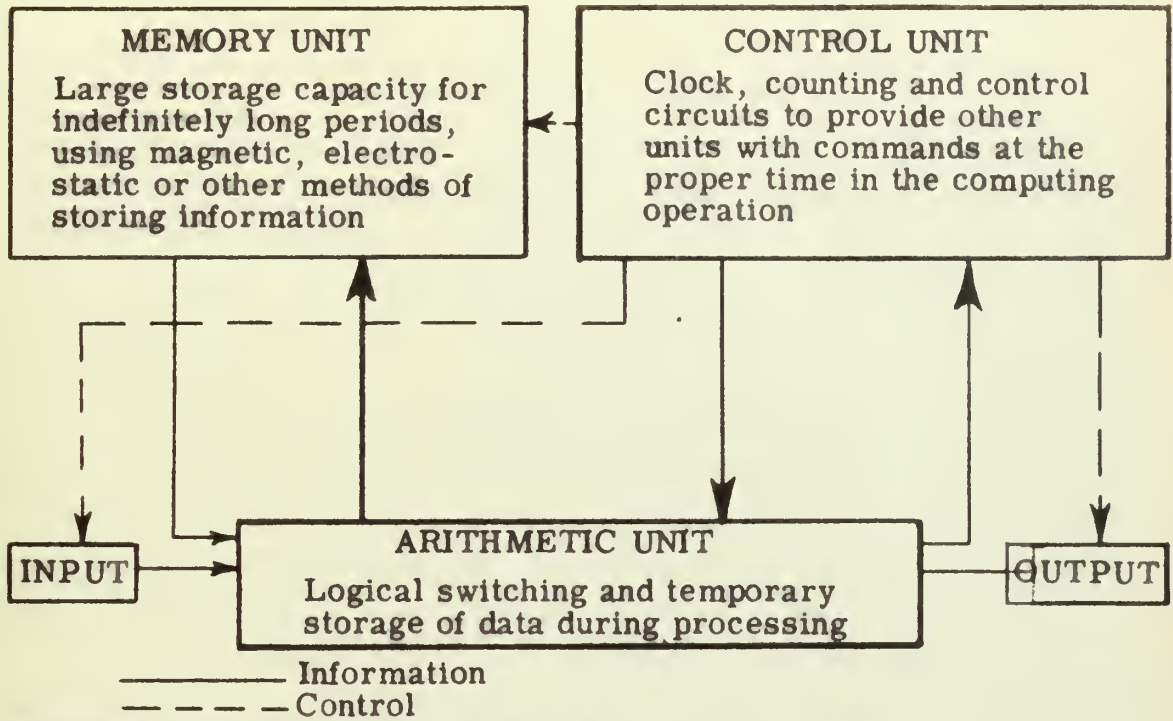the theoretical time required for $i_c(t)$ to reach 90% of its final value
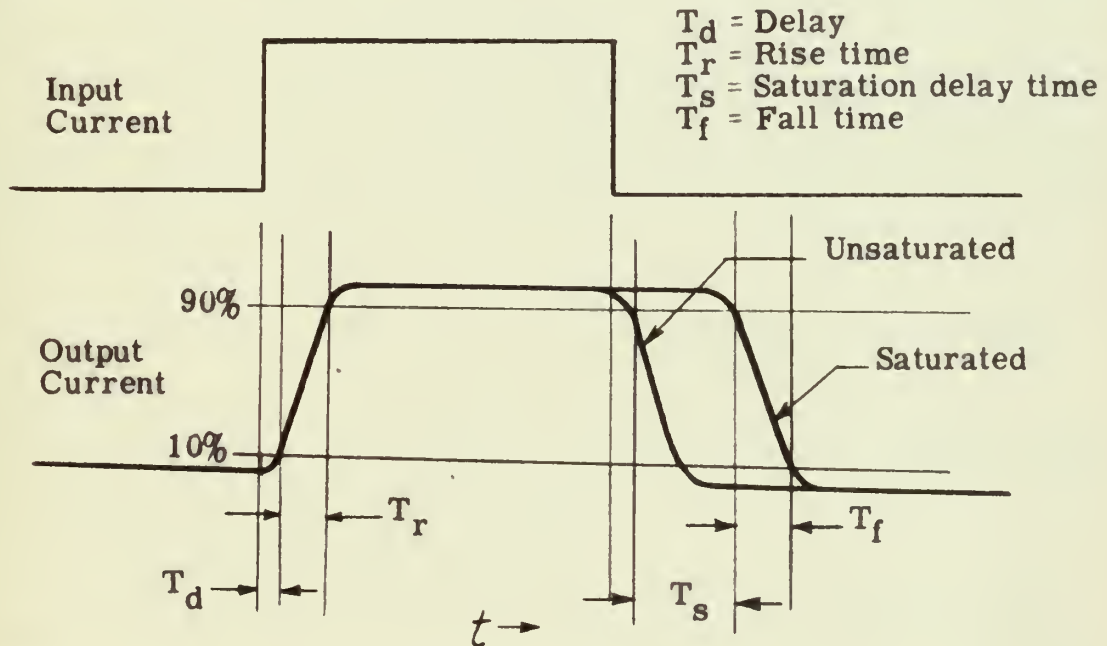
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Figure 2.1 Digital Computer Functional Operation

Figure 2.2.   Response of saturated and unsaturated circuits

4

becomes:

$$t_{.90} \cong \frac{.41}{f_{\alpha_{co}}} \qquad (2\text{-}2)$$

For $f_{\alpha_{co}} = 200$ mc, a reasonable value for the 2N501 diffused base transistor, $t_{.90}$ theoretically could be reduced to two mμseconds. Response is also dependent upon the circuit associated with the transistor, however, so that this ideal switching time cannot be realized in practice; but the importance of a very large alpha cutoff frequency is demonstrated.

Operation of the transistor in the saturated region results in slower switching speed due to an additional delay known as saturation delay time, T_S [3, 4]. This is shown in Figure 2.2. T_S becomes significant if an inherently slow transistor is used, auxiliary circuitry then being necessary to prevent saturation from occurring.

The collector voltage swing must also be considered in design of high speed switching circuits since the time required to charge and discharge stray capacitance is directly related to the difference in voltage levels. Sufficient spread must be maintained, however, to eliminate uncertainty in the logical circuits.

Finally, the input or driving signal should be made as large as possible to reduce T_{SW}, the switching time, as shown by Ebers and Moll [5]. An expression relating T_{SW} to input signal for the common emitter configuration is given in (2-3),

$$T_{SW} = \frac{1}{(1-\alpha_N)\omega_\alpha} \ln \frac{i_{B_{IN}}}{i_{B_{IN}} - .9\left(\frac{1-\alpha_N}{\alpha_N}\right)I_{CS}} \qquad (2\text{-}3)$$

where $I_{CS} \cong \frac{V_{cc}}{R_L}$, $\alpha_N = \frac{I_c}{I_e}(V_{cB}=0)$.

The faster switching time, obtained, however, must be weighed against the required increase in driving power.

c. Information Storage Circuits

One of the basic building blocks of a digital computer is a device that will store information and distinguish between input voltage levels which contain logical information. It is known as a register and must maintain the required state of current flow or output voltage associated with the logical levels employed in the system until the input voltage, or logical signal, switches it to another state. In a binary system, such
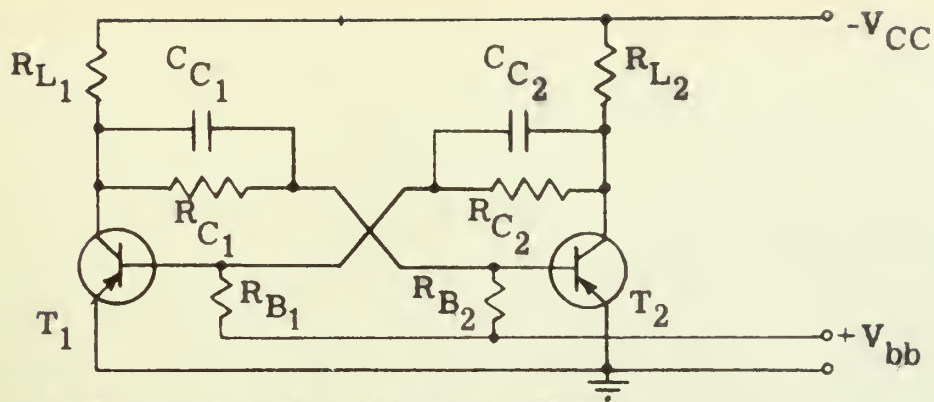
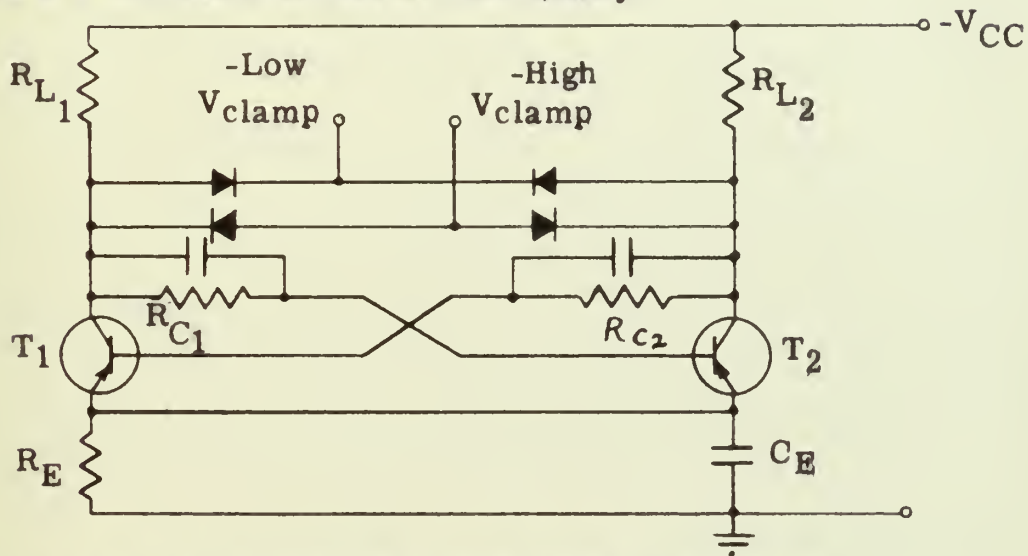Figure 2.3 Saturated Eccles-Jordan Binary

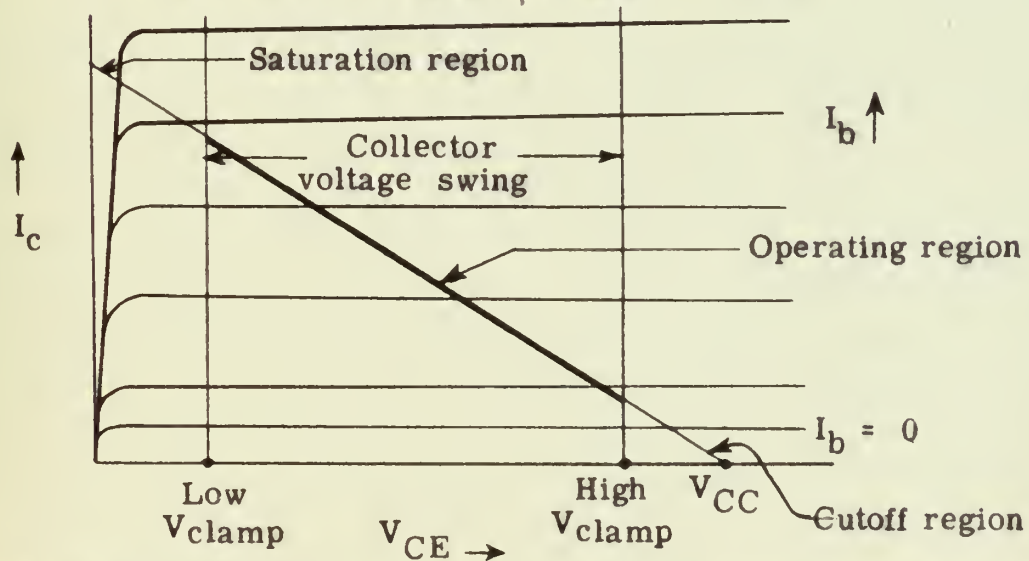Figure 2.4(a) Nonsaturating binary using diode clamps
with separate supply voltages

Figure 2.4(b) Effect of clamping on transistor characteristics

6

as the one being studied here, two levels are required and these can be represented by the saturated and cutoff collector voltages of the transistor or by the voltages associated with two different states in the active region of its operation.

The use of a saturated Eccles-Jordan binary for this function has been widely studied $\underline{/3/}$, the transistor circuit following logically from its vacuum tube predecessor. An example of this design is shown in Figure 2.3. A modification which prevents saturation in order to obtain higher switching speed is shown in Figure 2.4 (a). This configuration employs clamping diodes to limit operation to the active region as can be seen from the transistor characteristic curves in Figure 2.4 (b).

Development of transistors having low saturation voltage, small storage times and high $f_{\alpha co}$ made the direct coupling of stages both feasible and attractive; this approach is known as direct coupled logic, or DCTL $\underline{/6/}$. The binary is assembled by connecting the base of one transistor directly to the collector of the other, as in Figure 2.5, the saturation collector voltage of T_2 being low enough to maintain T_1 cutoff; this relation is expressed in (2-4):

$$\left| V_{CE} \text{ (saturated)} \right| \;<<\; \left| V_{BE} \text{ required to turn transistor on} \right| \quad (2\text{-}4)$$

The principal advantage of DCTL circuitry is simplification in design, which is readily seen by comparing Figures 2.3, 2.4 (a) and 2.5. Other advantages are low supply voltage, reduced power drain, and the need for only one value of supply voltage.

The storage units described above have the common property that switching from one state to another is accomplished by collector-to-base biasing networks. Another method of obtaining information storage is known as a two inverter toggle, which consists of two transistor stages in series, as in the block diagram of Figure 2.6. Once the input logical signal has set the toggle it may be removed since feedback from the second stage will hold the circuit. One possible circuit configuration is shown in Figure 2.7$\underline{/7/}$.

    d. Logical Switching Circuits or Gates

The gating or logical switching function performs the combination of signal voltages according to the requirements stipulated
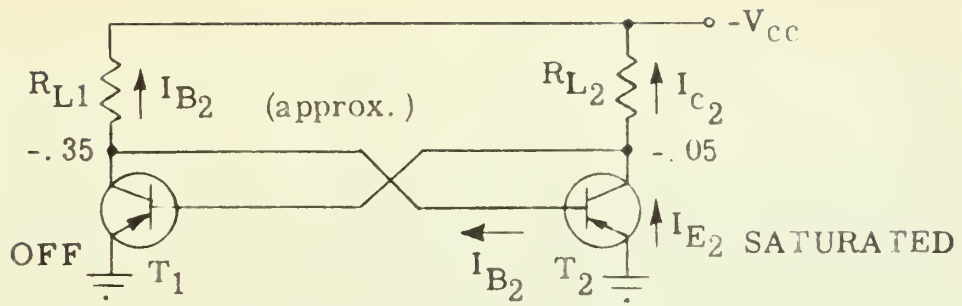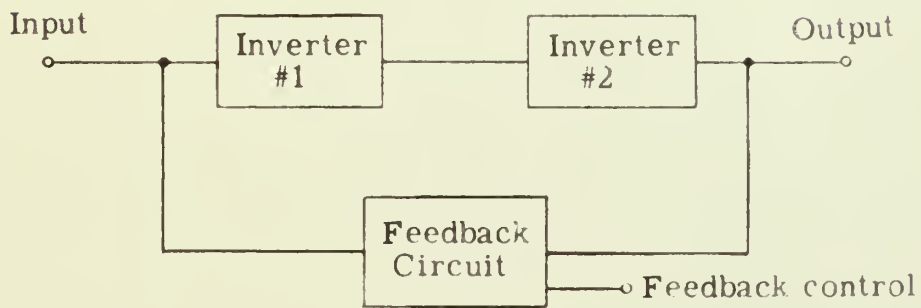
Figure 2.5.   Direct Coupled Transistor Circuit
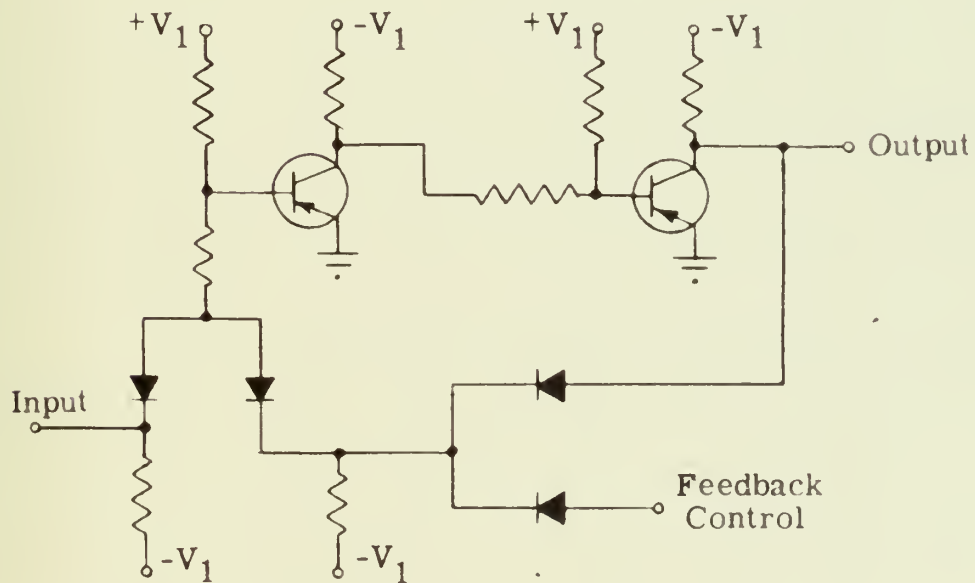

Figure 2.6.   Two Inverter Toggle

Figure 2.7.   Two Inverter Circuit

8

in the circuit design by the logical equations for the system. It can be accomplished by diode circuitry, a transistor network or transistor-resistor logic (TRL).

Transistor-resistor logic, or TRL $\underline{/8, 9\,\underline{7}}$, employs resistors as the primary component in the design of the switching circuit. Figure 2.8 shows a representative TRL configuration, switching of the nearly constant current sources (transistors) being accomplished by resistor networks and bias voltages. TRL is a straightforward approach and requires a relatively small number of transistors. However, resistor value tolerance and supply voltage regulation becomes critical if operation of the transistor must be confined to the active region, which is necessary if $f_{\alpha co}$ is low.

Use of diodes is one of the most common ways to obtain gating $\underline{/1\underline{7}}$, their wide selection at relatively low unit price making them an attractive computer component. Examples of diode gates are shown in Figure 2.9 in a system using 0 volts for the logical "0" and -2 volts for "1".

The characteristics of the transistor that facilitate the direct coupled circuits described above also make possible the design of gating circuits. The AND function is obtained by connecting the transistors emitter-to-collector, with output depending upon the energizing of all bases in the gate to provide current to R_L. The OR gate is effected by parallel connection, an output resulting if any one of the transistors is energized. Figure 2.10 shows typical arrangements.

e. Selection of Information Storage and Gating Circuitry for Study

From the foregoing discussion of design problems three systems were selected for study of performance and size capabilities using diffused base or drift transistors and/or high speed switching diodes; they are: (1) A direct coupled configuration, which employs transistors for the binaries and the logical switching circuits; (2) A transistor-diode system, using transistors for the storage functions and diodes for gating; (3) A transistor-resistor design, utilizing the TRL circuits described above. These three approaches are typical of circuitry suitable for computer systems and represent various degrees of compromise between cost, size and performance.
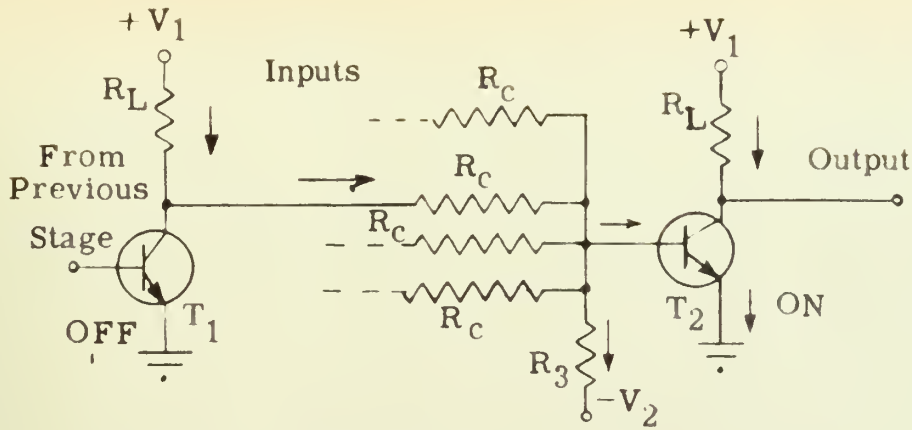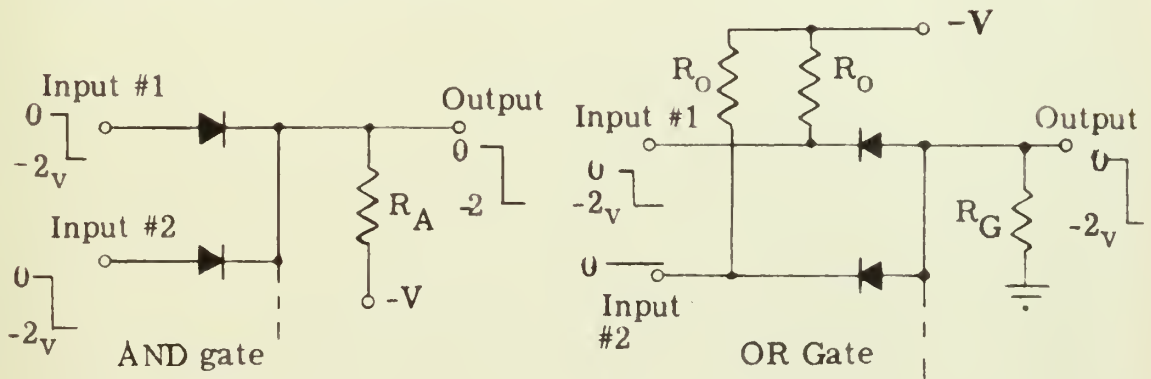
Figure 2.8. TRL Circuit

Figure 2.9. Diode Gates

Figure 2.10. Direct Coupled Transistor Gates
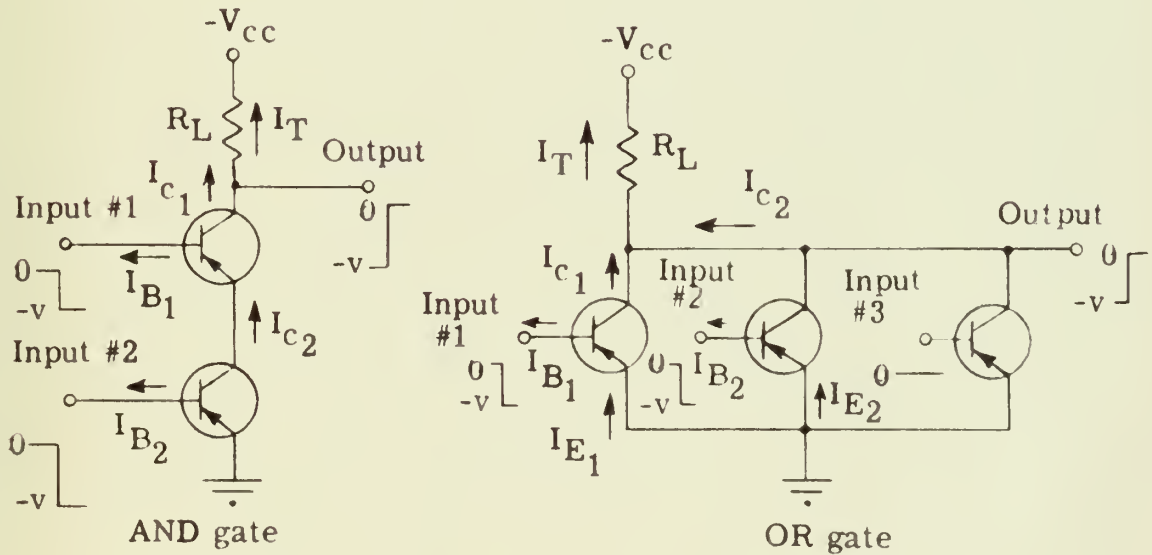
Diode and transistor selection for the study was made on the basis of switching capabilities and availability in production quantity, a necessity for computer applications. Included are the 2N501, 2N384 and 2N623 drift or diffused base type transistors as well as the S570G very fast switching diode. A summary of their more important characteristics may be found in Appendix I.

3. The Binary Adder Test System

The way in which the storage and switching circuits mentioned briefly in Section 2 are employed is determined by the purpose for which the computer is intended and the decision to use serial or parallel operation. In this paper the study was directed toward parallel operation because the ultimate application is a computer employing this type of system.

In the normal operation of a parallel adder the information flow would be, in general, as shown in Figure 3.1. The registers labeled A_0, A_1, ... A_N and B_0, B_1, ... B_N are set by the logical signals a_0, a_1, ... a_N and b_0, b_1, ... b_N, respectively. Each adder stage, except the first, combines the inputs from its A and B registers with the carry from the preceding stage to determine the final output sum and carry. In this manner the flow of information is propagated through the entire adder and consequently the output of the last stage is delayed by the time required for all the preceding stages to complete their operations. The performance of each stage must, therefore, be optimized if high speed operation is to be obtained.

The simulation of one-bit adder operation is accomplished by use of the test system shown in Figure 3.2. The pulse generator and complementing binary register provide the carry input. In this manner the input can be adjusted to duplicate the signal that would be used in normal adder operation and the delay and degeneration of the adder output signal may be measured.

The two logical levels required in the adder are provided by the output voltages of the binaries. The logical channels connecting the binaries to the adder are marked A_N, $\overline{A_N}$, B_N, $\overline{B_N}$, C_{N-1}, and $\overline{C_{N-1}}$, as shown in Figure 3.2. If the A_N channel is at the voltage associated with a "1", the bit, or binary digit, content of the A_N register is said to be "1" and the $\overline{A_N}$ channel will be at the voltage level associated with "0". In this manner the adder may be realistically operated by setting the desired voltage levels in the static A_N and B_N registers and having the C_{N-1} complementing binary output change as it is pulsed by the generator. The carry input to the adder is in this way changed at the switching speed of the C_{N-1} binary, simulating adder operation. Table I shows the possible logical combinations found in the adder.
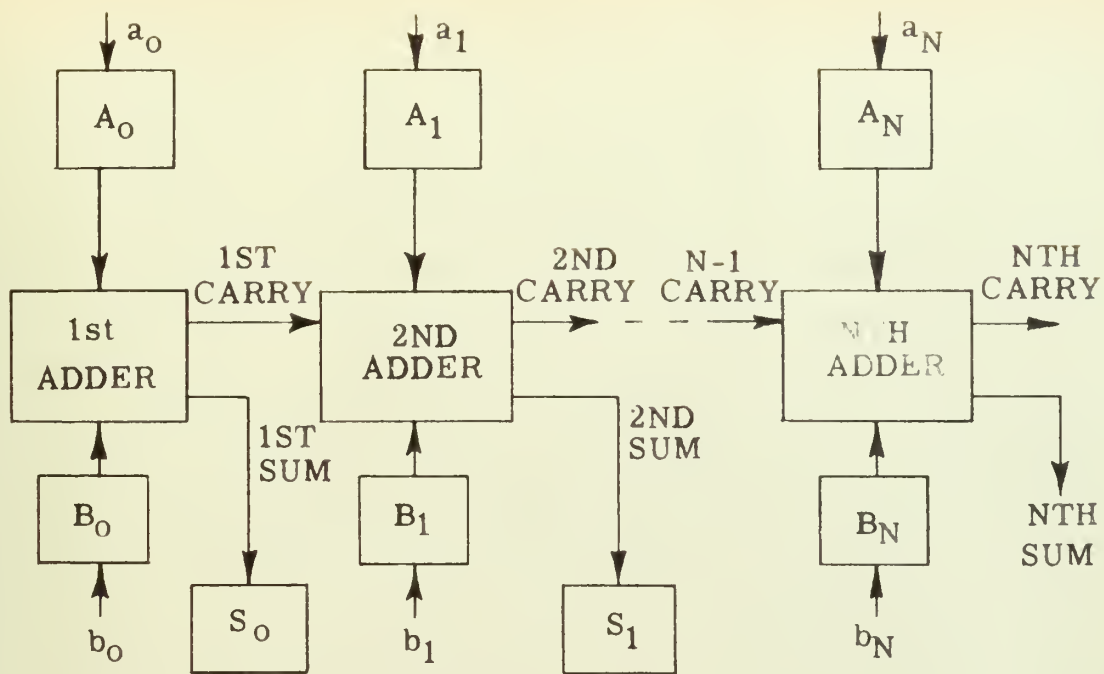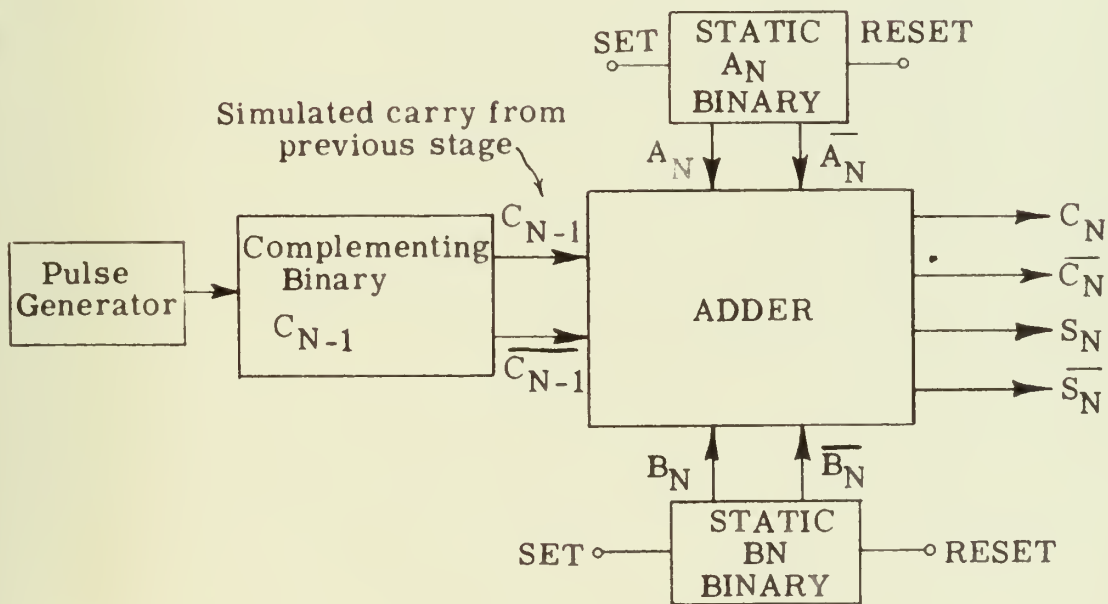
12

Figure 3.1. N-Stage Parallel Adder

Figure 3.2. Test System for One – Bit Adder

There are four equations that can be written to express the carry and sum outputs of the adder: C_N, $\overline{C_N}$, S_N and $\overline{S_N}$. This development is carried out in Appendix II and one possible configuration of the adder as derived from the equations, is shown in the block diagram of Figure 3.3. The existence of a preliminary sum is indicated by the S_N' and $\overline{S_N'}$ channels in the diagram. The combination of the C_{N-1} and $\overline{C_{N-1}}$ carry signals with this preliminary sum determines the output of the adder.

The circuitry required to perform the logical functions represented by the equations of Appendix II were designed for the three systems described in Section 2.e, their evaluation and comparison being carried out in subsequent sections of this report.

Switching mode numbers		1	2	3	4	5	6	7	8
Inputs from Registers	A_N	0	1	0	1	0	1	0	1
	B_N	0	0	1	1	0	0	1	1
	C_{N-1}	0	0	0	0	1	1	1	1
Adder Outputs	C_N	0	0	0	1	0	1	1	1
	S_N	0	1	1	0	1	0	0	1

Table I Logical inputs and outputs of the binary adder


Figure 3.3 Adder logical diagram

4. Pulse Generation Circuits

In order to simulate the operation of the adder circuits a pulse source is necessary to drive the C_{N-1} complementing binary, as described in Section 3. This function may be obtained with any one of several types of pulse systems, using the diffused base or drift transistor for high prf capability. Considered were a monostable multivibrator, an astable multivibrator, and a blocking oscillator-pulse shaping circuit. While the multivibrators were considered satisfactory, the blocking oscillator system was selected for this study because it provided convenience of control over a wide range of prf and pulse width.

Design of the blocking oscillator was based on a version suggested for the 2N501 transistor [9]. This circuit was modified for use with a 2N384 transistor to take advantage of the latter's higher maximum V_{CE} rating. The value of R_C was adjusted to prevent I_C (Max) from being exceeded. The circuit is shown in Figure 4.1 with a photograph of the output waveforms at 1, 5 and 10 mc. Three frequency ranges could be selected by switch S_1, exact prf desired being adjusted with the variable capacitor C_E and 150K potentiometer. The blocking oscillator provided a stable pulse source from less than 1 mc to about 12 mc, pulse width varying from approximately .05 to .70 μ seconds depending on prf.

The shaping stages of the pulse generator consist of two overdriven amplifiers, or inverters, with an additional emitter follower stage included to provide oscilloscope synchronization, as shown in Figure 4.2. Output pulse width was varied by adjusting base resistor R_1 to control the extent to which the first inverter stage saturated. For amplitude control a 2N501 emitter follower stage, such as that shown for the sync amplifier, is employed after the second inverter. Load resistances were made as small as possible for fast rise time, the 2N501 being selected for use in the pulse output stage because of its very high I_C (max) of 50 ma. Typical waveforms at approximately 2.5 mc are included with the circuit diagram.
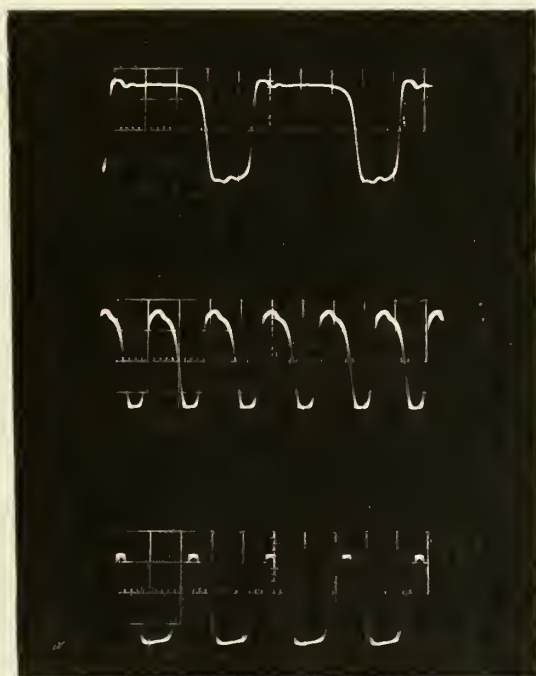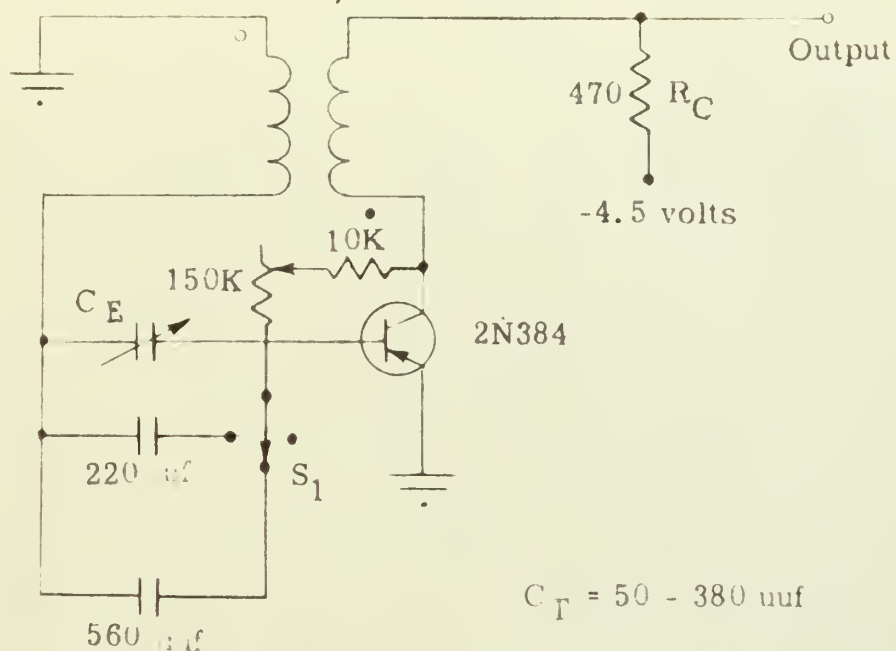
Figure 4.1   Blocking oscillator with representative waveforms
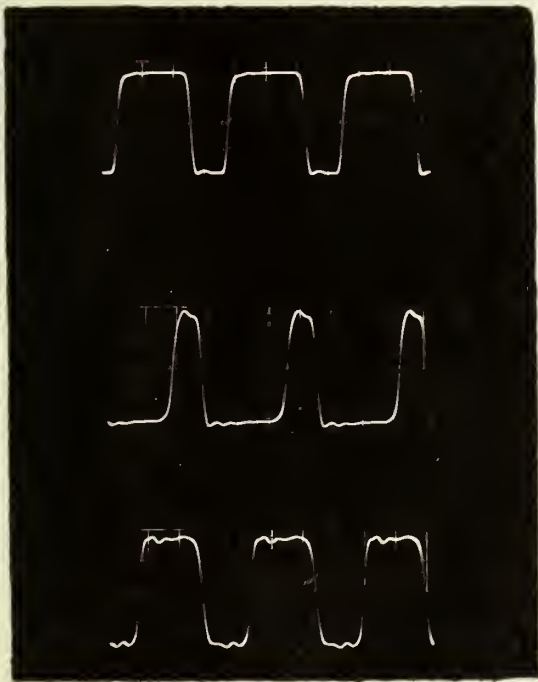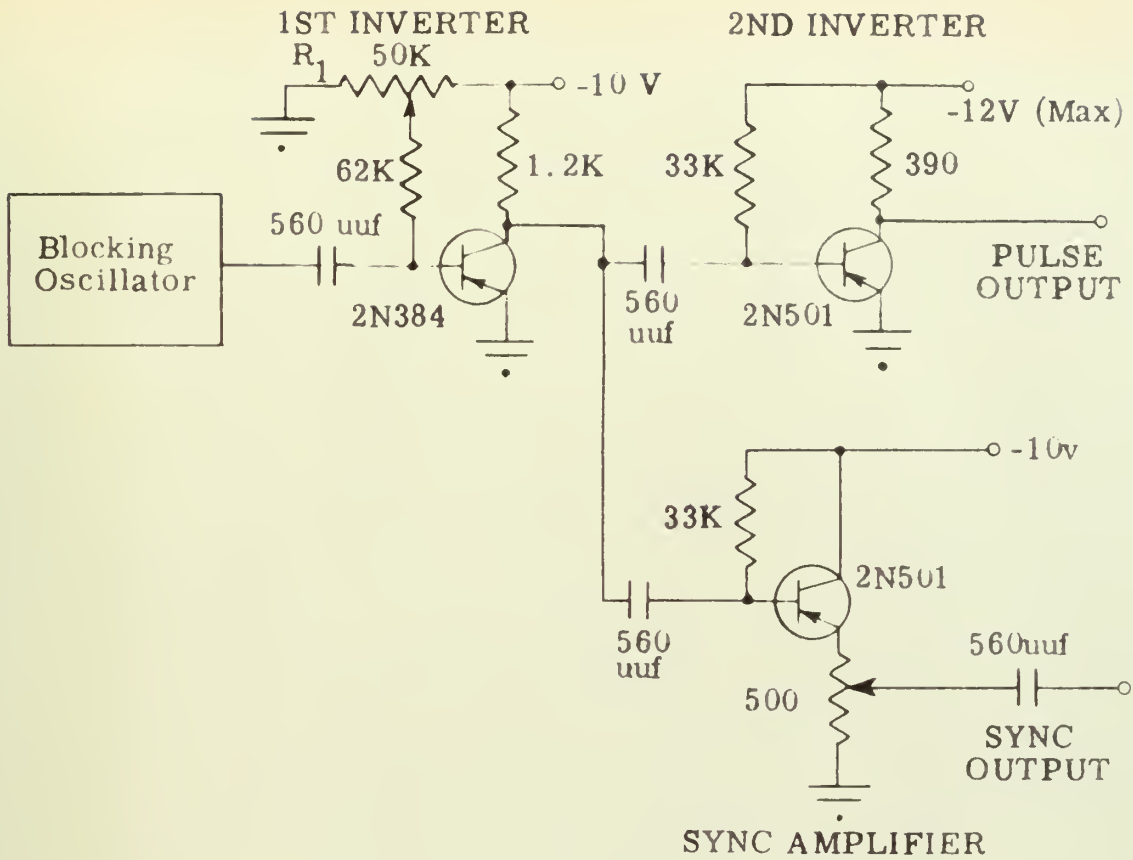
Figure 4.2. Pulse Shaping Stages With Typical Waveforms at Approximately 2.5 Megacycles

18

5. The Direct Coupled Binary Adder

The characteristics of certain transistors that make possible the direct connection of base to collector in binary circuits were described in Section 2. The use of transistors for gating circuits was also discussed. This direct coupled system, or DCTL, not only eliminates many of the components normally required in binary and logic circuits but operates with a very low supply voltage, an important consideration in computers where hundreds of transistors are employed.

The complementing binary required for C_{N-1} simulation is obtained by adding an input steering network to the circuit of Figure 2.5 so that pulses with high prf will cause it to change state. The steering function may be designed with transistors or diodes; one possible configuration, employing transistors, is shown in Figure 5.1. This binary functioned satisfactorily over a wide range of prf's, the highest value being ten mc with a driving pulse amplitude of 12 volts. The input pulse amplitude required for reliable operation varied from four volts at one mc to 12 volts at ten mc. Photographs of the binary input and output waveforms at switching frequencies of one and 6.2 mc are shown in Figure 5.2. The output f_{sw} of the complementing binary is just half of the input prf from the pulse generator, which is obvious from the photographs. Values of R_B, C_{in} and C_B depended upon switching frequency and pulse width.

The adder circuitry was designed with the gates described in Section 2 combined to obtain the necessary logical operations. Inspection of Figure 3.3 indicates that 14 two-input gates requiring 28 transistors are required for the adder. This number may be reduced substantially by simplification of circuitry (see Appendix II) and by utilizing certain transistors to perform more than one function. The resulting direct coupled adder design is shown in Figure 5.3.

The input voltages to the adder are the collector voltage levels of the registers, which are approximately -.05 and -.40 volt for the direct coupled design. In the tests of the adder's switching capability the A_N and B_N registers (see Figure 3.2) were statically set and the C_{N-1} register was switched by the complementing input signal from the pulse generation circuits described in Section 4.

Since the slowest carry propagation time in the adder determines the maximum switching speed at which the adder can operate, the design and performance study must include all the possible modes of operation.
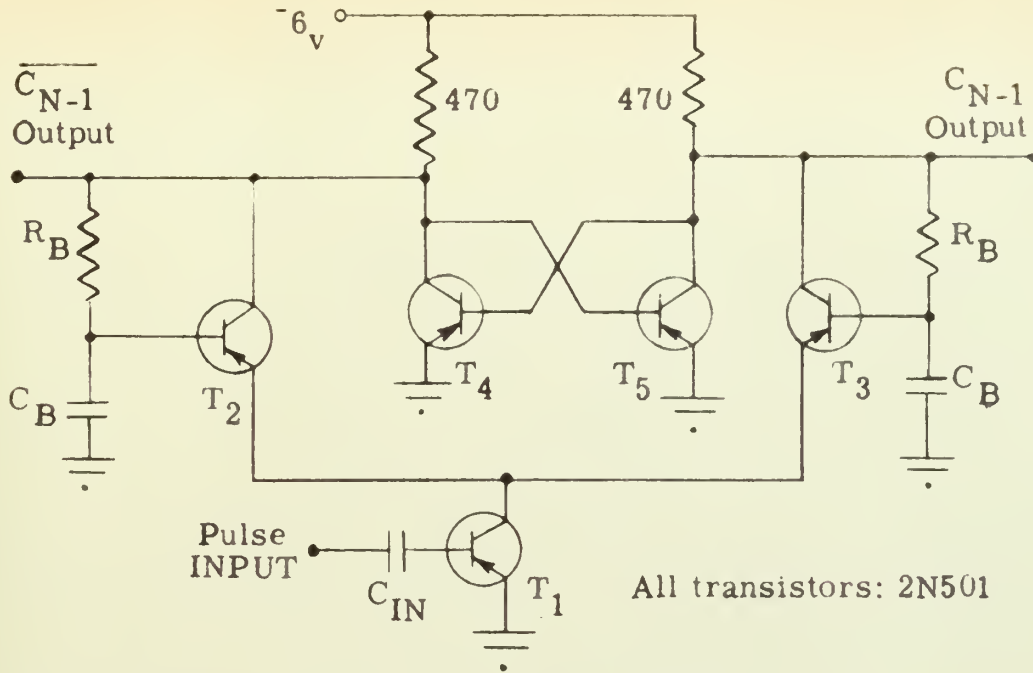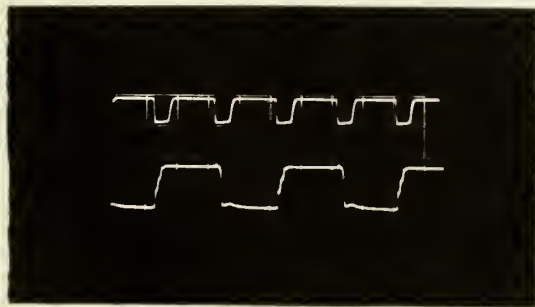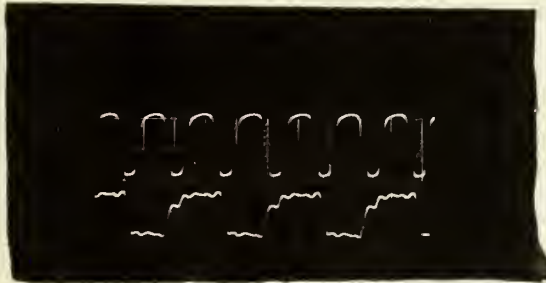
Figure 5.1. Complementing Direct Coupled Binary With Transistor Steering Network for C_{N-1} Carry Simulation

$f_{sw} \cong 1.0$ mc

Upper : Input
0.5 usecs/div
5.0 volts/div

Lower: Output
0.5 usecs/div
0.5 volts/div

$f_{sw} \cong 6.2$ mc

Upper : Input
0.1 usecs/div
5.0 volts/div

Lower: Output
0.1 usecs/div
0.5 volts/div

Figure 5.2. Photographs of the Input and Output Waveforms for the C_{N-1} binary of Figure 5.1

ALL R_L = 330 Ω
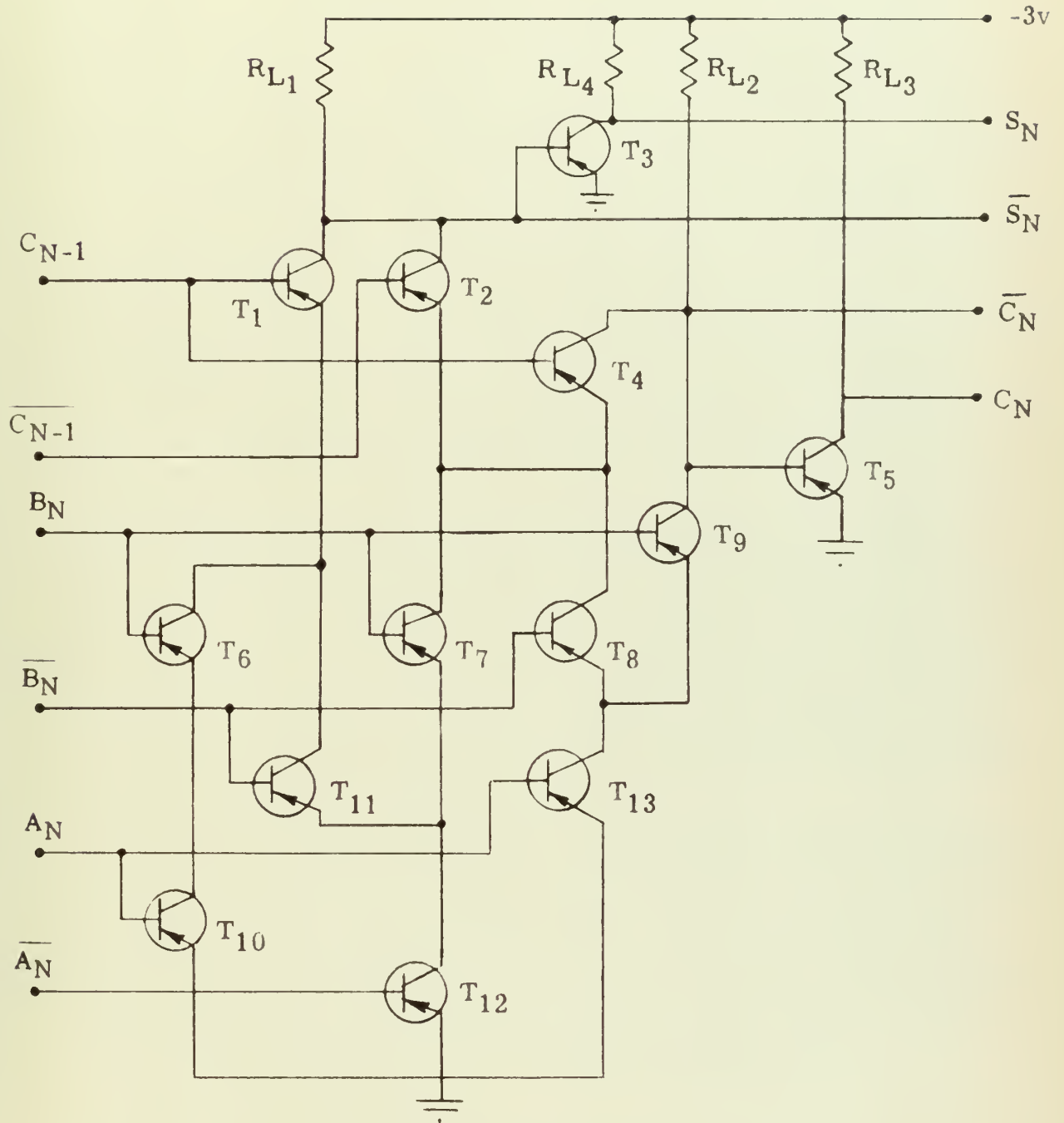
All transistors: 2N501

Figure 5.3. Direct Coupled Adder

Table I shows the eight different ways that the adder circuits can be set and assigns mode numbers to them for identification. Inspection of this table shows that carry propagation is affected only in the 2-6 and 3-7 mode combinations, as the C_{N-1} input is changed. It is sufficient, therefore, in this study, to investigate only the propagation delay times for the 2-6 and 3-7 mode combinations. T_P for these modes varied from 11 to 24 mμseconds, complete results being plotted in Figure 5.4 as a function of C_{N-1} input rise time, T_r. Switching frequency was varied from 0.5 to 5.0 mc.

The propagation delay time was measured from the 50 percent point on the leading edge of the input waveform to the identical point on the output waveform, as shown in Figure 5.5.

Power consumption for the DCTL adder (Figure 5.3) was 66 milliwatts. The circuit was assembled without special selection of components and supply voltage was reduced .72 volt and increased 8.0 volts or more with no adverse effect on operation. The design in Figure 5.3 shows that 13 transistors and four resistors were necessary.

Investigation of the adder's high speed performance and propagation delay time was carried out with a Tektronix type 541 oscilloscope, using the type 53/54C dual-trace preamplifier. The dual output as well as syncronization circuitry employed in the adder evaluation is shown in Figure 5.6. In order to obtain permanent records of the adder's operation for comparison and analysis, photographs of the waveforms were taken with a Dumont type 302 camera. Representative samples are shown in Figure 5.7.

The main advantages of the direct coupled circuits that are applicable to the packaging problem have been demonstrated previously--they require fewer components and relatively low power. There are several basic considerations necessary in the design process, however, that affect the final packaging configuration; these may be outlined briefly as follows:

(1) Will the system be subjected to extreme shock, vibration or handling conditions and will there be unusual temperature variations?

(2) Is there an optimum building block size that may be determined from analysis of system application requirements?

In (2) the equipment in which the computer is to be installed as well as maintenance and repair philosophies must be taken into consideration.
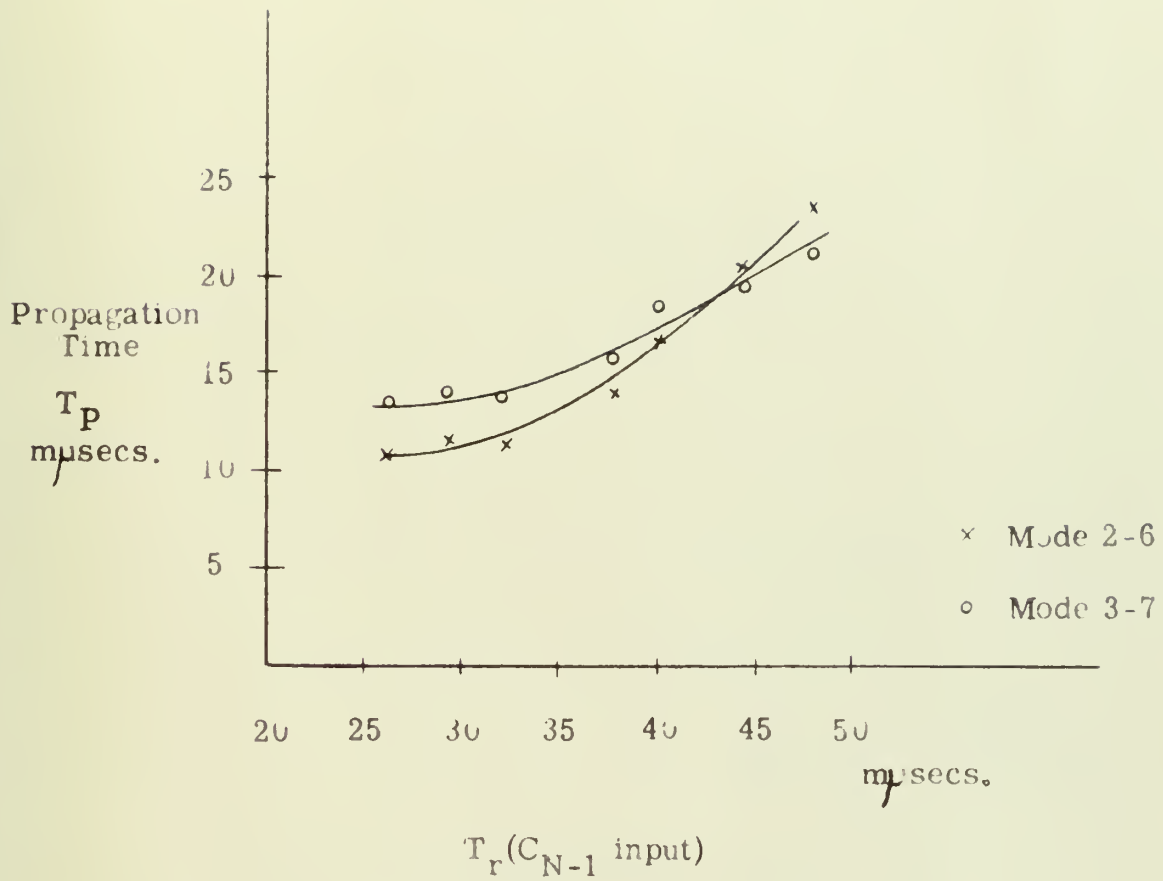
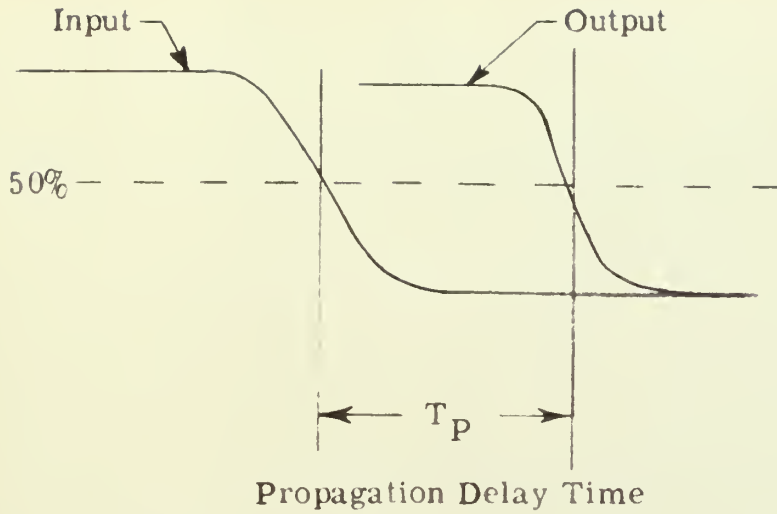Figure 5.4. Propagation Delay vs. T_r for the Direct Coupled Adder

Input ⟶

Output ⟶

50% ⟶

T_P

Propagation Delay Time

Figure 5.5 Definition of Propagation Delay Time

Set ⚬ ⚬ Reset

A_N Binary

A_N $\overline{A_N}$

Tektronix
Type 541
Oscilloscope

Blocking
Oscillator

Pulse
Forming
Circuits

Complement-
ing
Binary
C_{N-1}

Direct
Coupled
Binary
Adder

C_N
Out
put

Sync
Amplifier

B_N $\overline{B_N}$

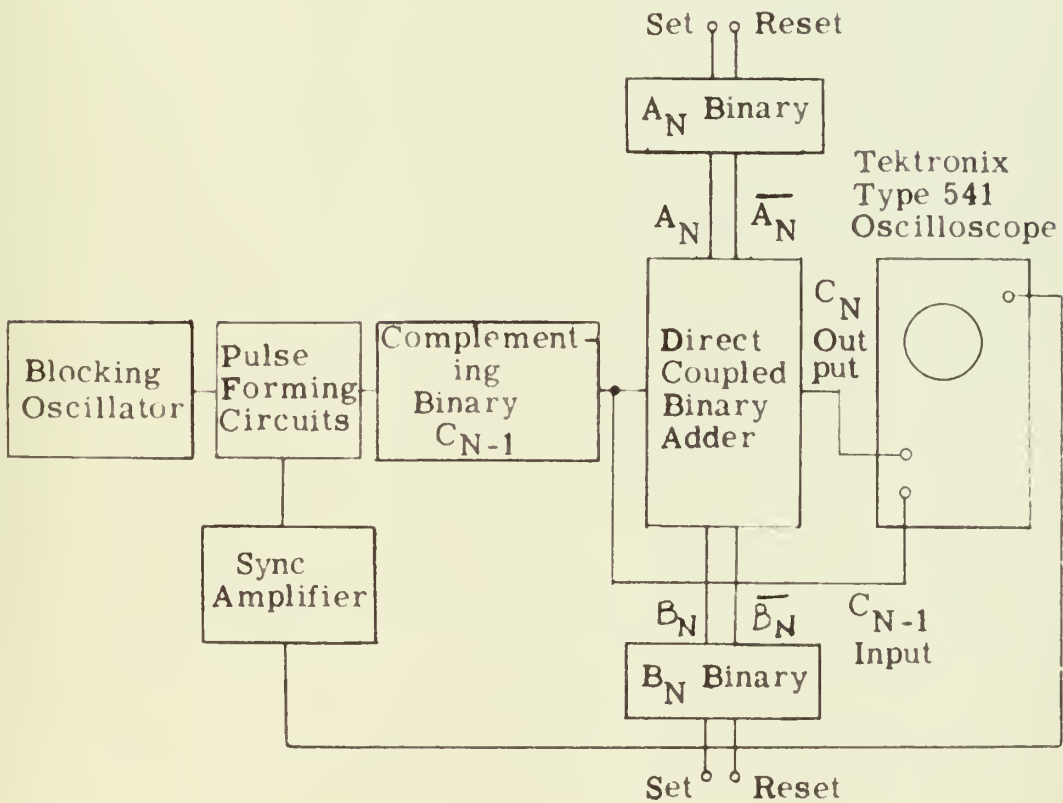C_{N-1}
Input

B_N Binary

Set ⚬ ⚬ Reset

Figure 5.6. Adder Test Equipment and Arrangement

24

With these points in mind the designer might approach the problem in a manner similar to that shown in Figure 5.8, which is a scaled photograph of the adder circuitry. This design is a breadboard prototype intended to fit into a standard twelve terminal printed circuit plug-in board; it includes the thirteen transistors in the adder circuit and one additional for indicator operation, if necessary.
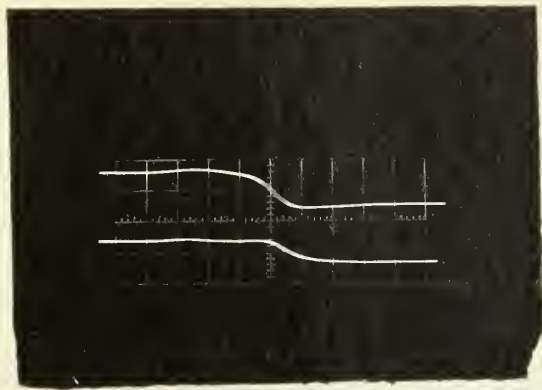
$f_{SW} = 0.5$ mc

Upper waveform: C_{N-1} input

Lower waveform: C_N output

Horiz. scale: .02 usecs./div

Vert. scale: .5 volt/div

T_p 12 musecs.; T_r 32 musecs.

$f_{SW} = 3.5$ mc

Upper waveform: C_{N-1} input

Lower waveform: C_N output

Horiz. scale: .02 usecs./div
Vert. scale: .5 volt /div

T_p 14 musecs.
$T_r = 32$ musecs.

Figure 5.7. Photographs of typical direct coupled adder input and output waveforms for propagation delay time measurement; mode 2-6.
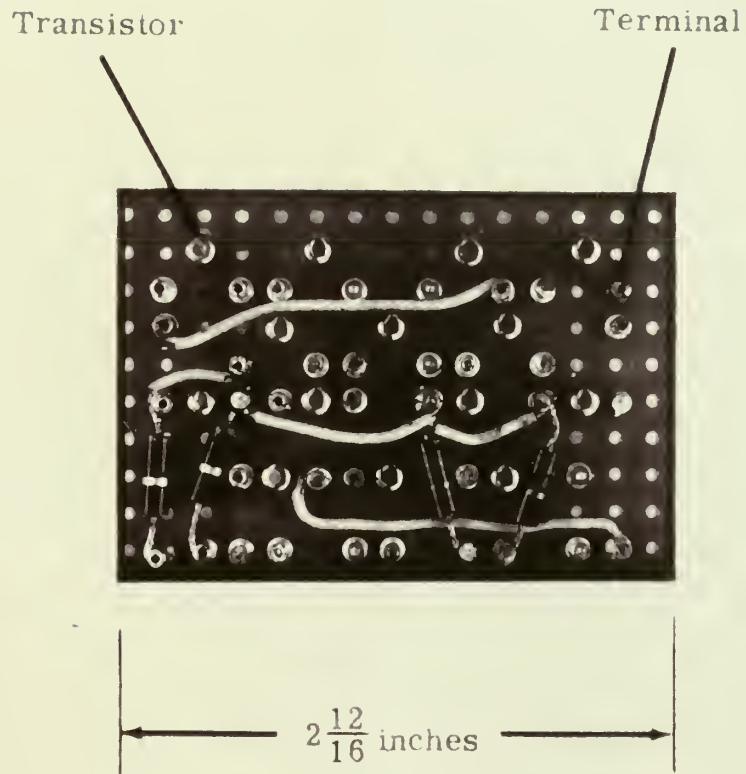
Transistor   Terminal

$2\frac{12}{16}$ inches

Figure 5.8. Photograph of Direct Coupled Adder Packaging

6. The Switching Diode Binary Adder

Use of diodes in the logical circuitry allows the elimination of a large number of transistors compared with the DCTL design, as may readily be seen from the brief discussion of this configuration in Section 2. The advent of high speed semiconductor diodes has made this approach to the design problem even more attractive.

The design of logical switching circuits employing diodes is accomplished by one of several gating methods $\boxed{1}$, using AND and OR gates described previously to obtain the switching functions required by the logical equations (see Appendix II). One possible configuration of the full binary diode adder design is shown in Figure 6.1.

Unlike the direct coupled system, the difference in output voltage levels of the binary which drives the diode circuits is preferably large to avoid ambiguity. In addition, the diode design uses four voltage levels, the two associated with the logical "1" and "0" signals and two bias voltages, V_H and V_L. Consequently, the binary circuit was designed with the 2N623 transistor, which has a higher saturation voltage (see Appendix I). In this way the cutoff and saturation voltages of the binary could be employed as the "1" and "0" signals and ground represented the V_L bias voltage, only one additional bias voltage being necessary for V_H. The binary used to simulate the S_N' input is shown in Figure 6.2. The C_{N-1} input to the adder was obtained by driving a 2N623 emitter follower stage with the pulse generator, the output voltage levels representing the logical "1" and "0" for the diode logic. This circuit is shown in Figure 6.3. The C_{N-1} waveform was adjusted by means of the pulse generator controls and the 250K potentiometer in the 2N623 base circuit.

The measurement of pulse propagation time for the diode adder was accomplished by the test circuit shown in Figure 6.4. A type S570G high speed switching diode was selected for this circuit on the basis of its extremely fast recovery time of two mμ seconds (see Appendix I). The test configuration represents the stages in the adder that the carry pulse must propagate through. Diode D_1 is connected to the carry input from the previous stage, C_{N-1}, as described in Section 3; diode D_2 is connected to resistor R_3 and the output of a 2N623 binary set for a logical "1" to simulate the effect of the other AND gate input.
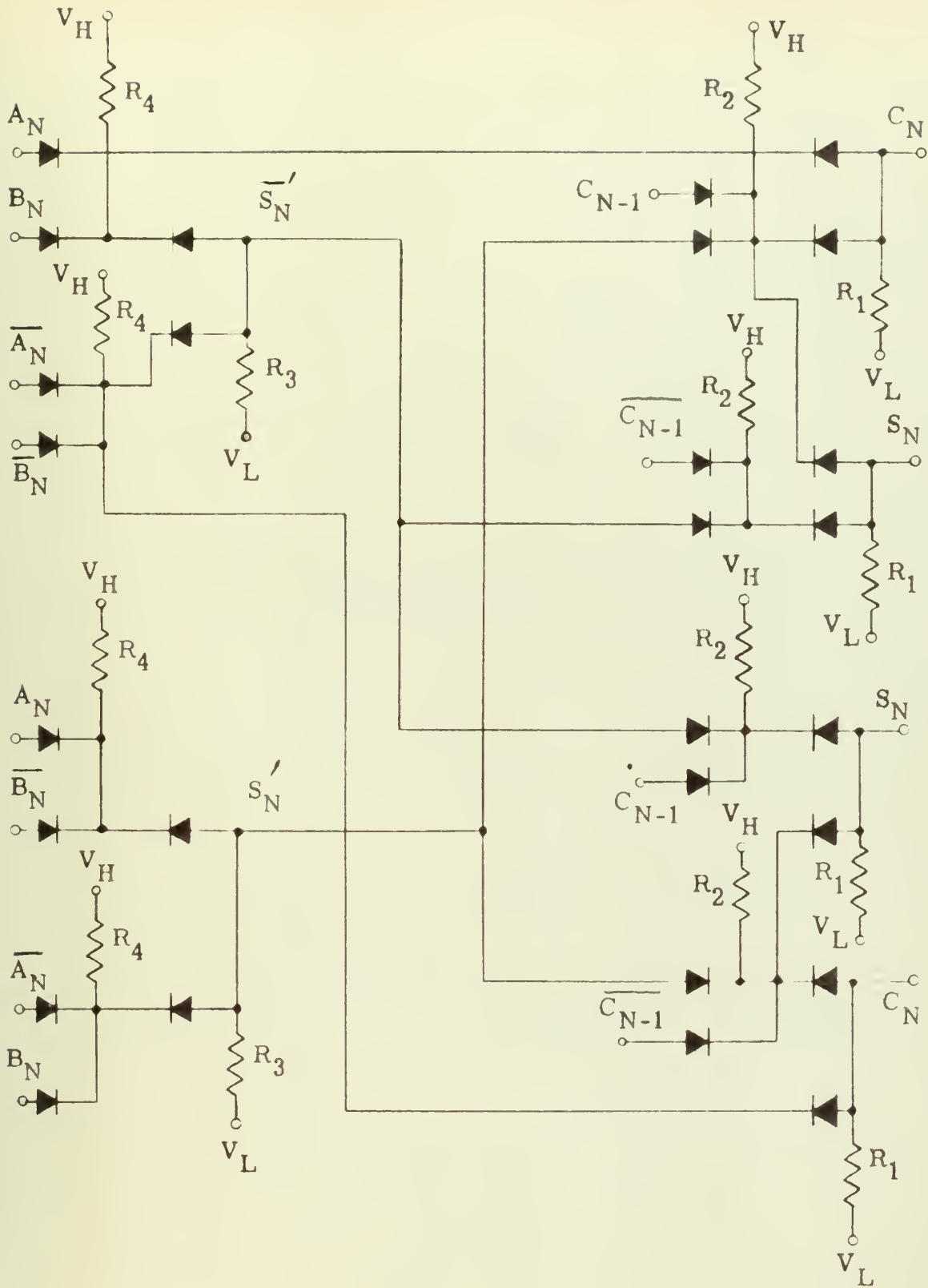
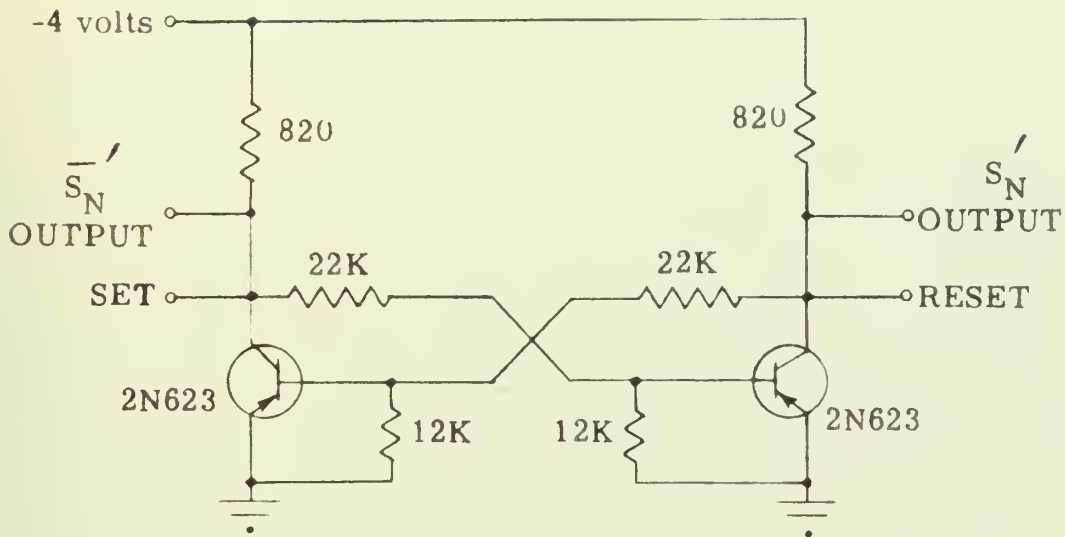Figure 6.1. The Diode Adder Circuit (Ideal)

29

Figure 6.2. The 2N623 Binary for S_N' Signal Simulation
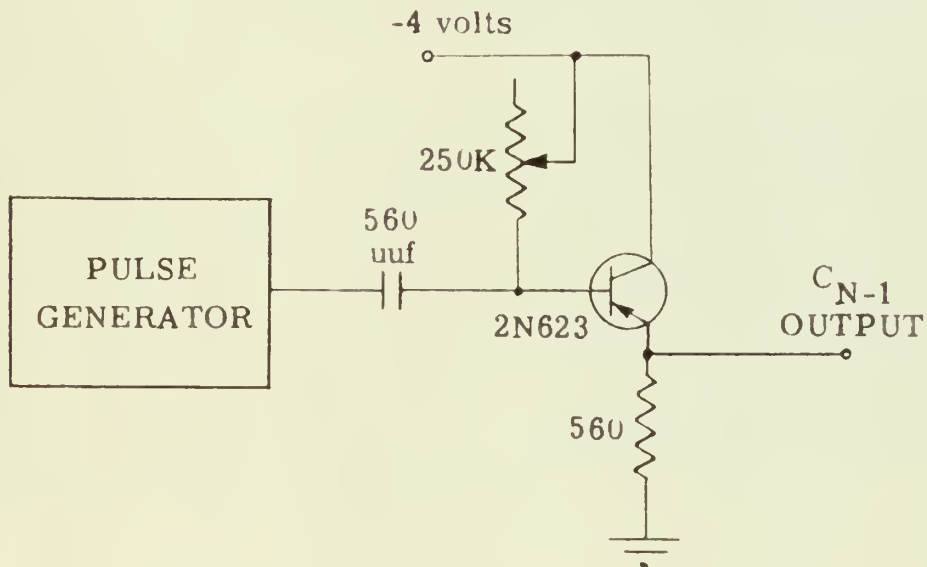in the Diode Adder

Figure 6.3. The C_{N-1} Input Signal Circuit for the Diode Adder

The propagation times obtained with the circuitry of Figure 6.4 ranged from approximately 12 to 18 mμ seconds, the switching frequency being varied from 1.0 to 8.5 mc. The variation in propagation delay time with T_r, C_{N-1} rise time, is plotted in Figure 6.5 and photographs of the input and output waveforms are shown in Figure 6.6.

The simulation circuit of Figure 6.4 represents an ideal configuration which is not valid for comparison with the other systems. In a realistic four-level diode logic circuit a stage of current amplification normally is required after every two levels [1], an additional carry propagation delay being introduced. The pulse propagation time for this additional transistor stage made the total variation in delay for the diode circuits approximately 26 to 40 mμ seconds. This is plotted in Figure 6.5 also.

Including power required by the current amplifier stages, the diode adder of Figure 6.1 operates at approximately 204 milliwatts. It was found that adjustments in the design values of components and supply voltages were necessary in these circuits due, primarily, to the difference in predicted and actual effect of the diodes on circuit parameters. In operation supply voltage variation of 25% or more could be tolerated, although a system with a small voltage difference in logical signals would probably require closer regulation for unambiguous operation.

The packaging problems and considerations present in the diode adder are basically quite similar to those outlined in Section 5 for the direct coupled circuits. Comparison of the diode adder circuit (Figure 6.1) with the direct coupled transistor configuration (Figure 5.3) shows the increased number of components required in the former—28 diodes and 14 resistors—and the need for current amplifiers makes the diode design even larger. Consequently the volume requirement of the diode circuits is estimated at approximately three times as great as the DCTL configuration pictured in Figure 5.8.
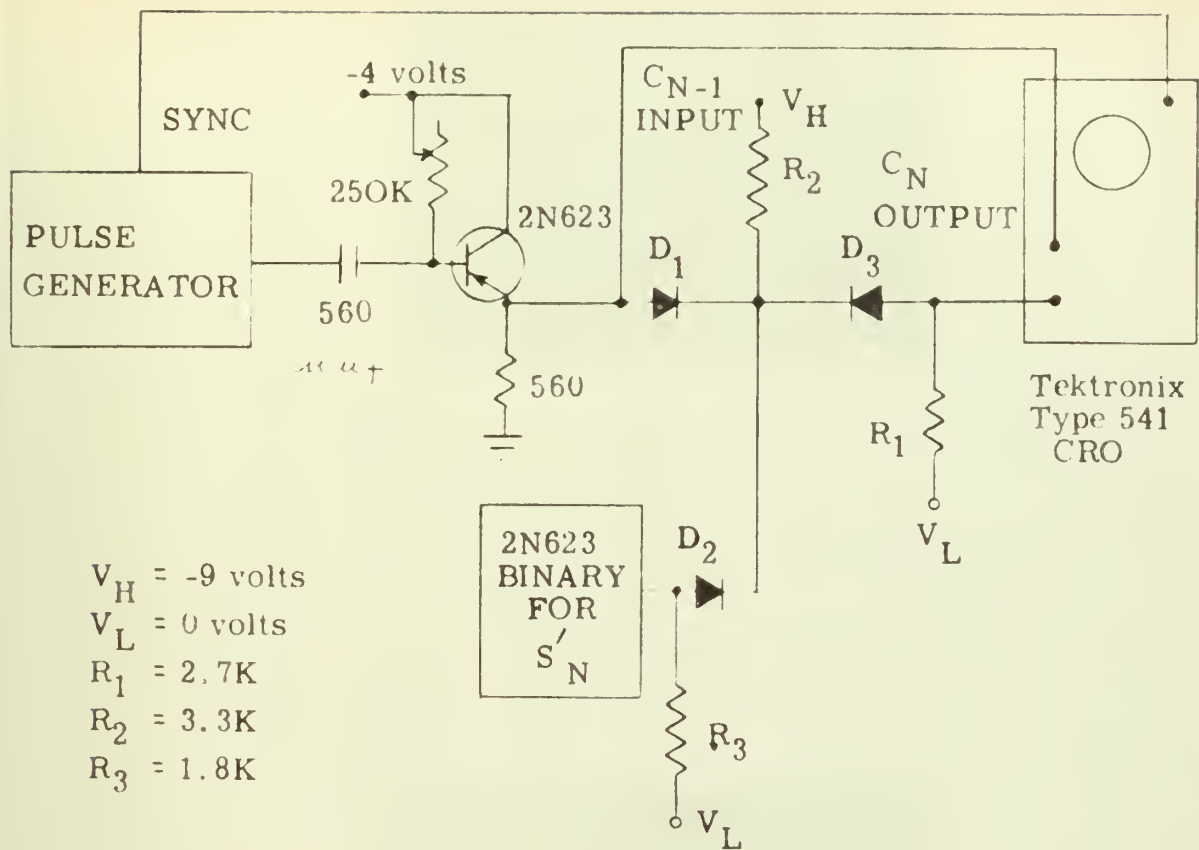
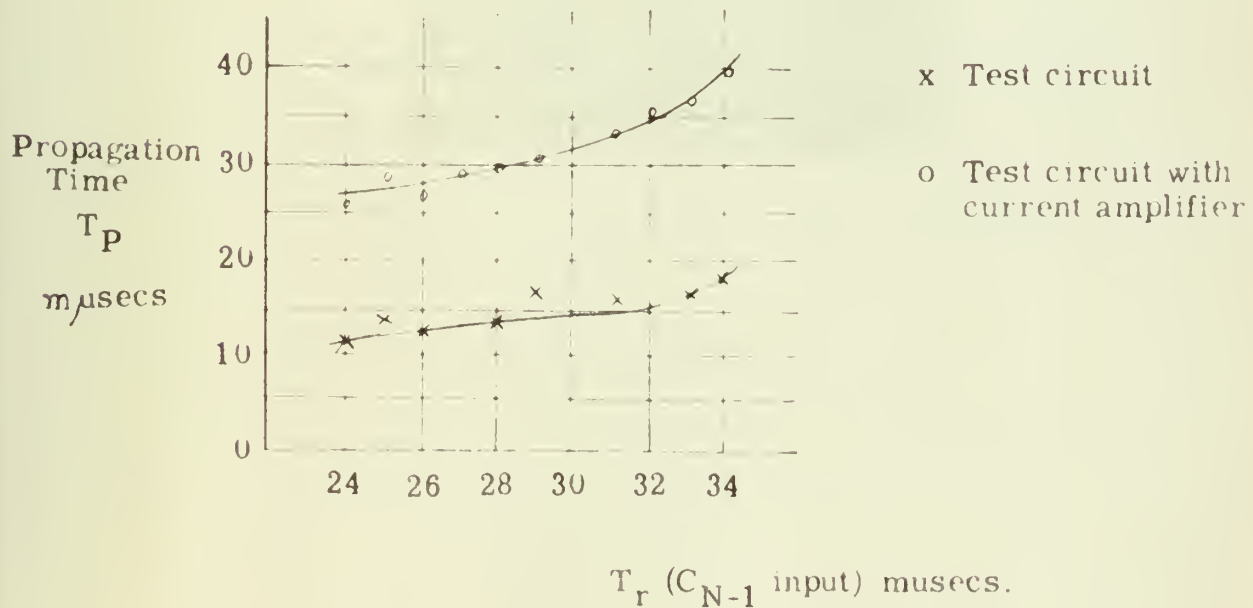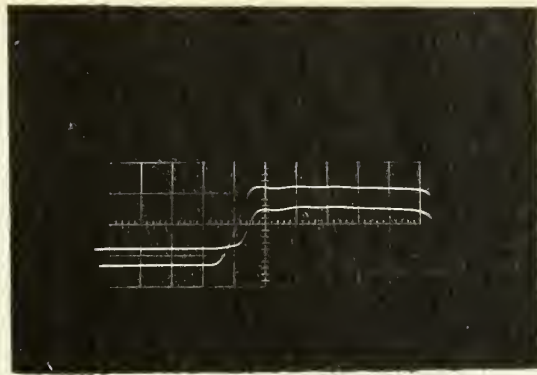Figure 6.4. Test Circuit for Pulse Propagation Time Measurement

V_H = -9 volts
V_L = 0 volts
R_1 = 2.7K
R_2 = 3.3K
R_3 = 1.8K

Figure 6.5. T_P vs. T_r for the Diode Adder

$f_{SW} \cong 1.7$ mc, Horiz. scale: .04usec div

Upper waveform:
      CN-1 input
      Vertic. scale: 1 volt/div
Lower waveform:
      CN output
      Vertic. scale: 2 volts div

$T_r \cong 32$ museconds

$T_p \cong 16$ museconds
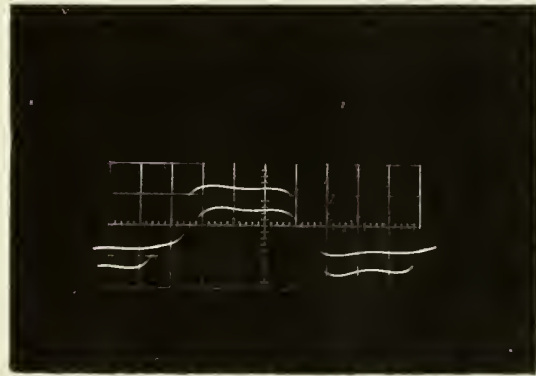
$f_{SW} \cong 6.0$ mc, Horiz scale: .02 usec div

Upper waveform:
      CN-1
      C_{N-1} input
      Vertic. scale: 1 volt div
Lower waveform:
      C_N output
      Vertic. scale: 2 volts div

$T_r \cong 26$ museconds

$T_p \cong 13$ museconds

Figure 6.6. Photographs of C_{N-1} and C_N waveforms for the test circuit of Figure 6.4

7. The Transistor-Resistor Logic Binary Adder

The switching circuitry described and tested in Sections 5 and 6 was designed with either transistors or diodes as the basic switching devices; i.e., the condition of the transistors—saturated or cutoff— and the biasing of the diodes in the logical circuits was utilized to obtain the necessary switching function. The transistor—resistor logic system employs resistors to realize the desired switching by controlling current flow in the network, transistors being used as the current sources $\boxed{8,9}$.

Design of the TRL circuits is carried out in the same manner as discussed in the DCTL and diode systems, using the logical equations of Appendix II. One possible configuration of the TRL adder that may be obtained from the equations is shown in Figure 7.1, with the basic gate circuit that requires only transistors and resistors depicted below. This gate can be employed for either AND or OR function by proper assignment of logical values to the voltage levels, the number of inputs depending upon requirements of the logic. In order to compare the TRL configuration with the DCTL and diode systems studied in Sections 5 and 6, the circuit in Figure 7.2 was designed, carry propagation time being measured as shown in Figure 7.3.

The test circuit of Figure 7.2 represents two levels of TRL logic, which simulates the actual propagation path that the carry pulse would follow in the adder. The C_{N-1} input consists of the complementing direct coupled binary described in Section 5 driving a 2N501 amplifier stage. The A_N and B_N signals to the AND gate are taken from amplifier stages T_2 and T_3, which are held in the saturated condition to obtain the low voltages that represent logical "1" inputs. The OR gate inputs consist of the AND gate output and a grounded 1.5K resistor, which constitutes the "worst condition" of the other three AND gates having a logical "0" output. Thus, as the C_{N-1} transistor (T_1) is switched by the complementing binary, the output of the AND gate turns transistor T_4 on and off. This, then, provides the input to the OR gate and the C_N output of the adder is obtained at the collector of transistor T_5.

The propagation time for the TRL circuit was found to be considerably longer than that of the diode and direct coupled systems. A plot of T_P as a function of the rise time of the C_{N-1} input, T_r, is shown in Figure 7.4. The propagation time varied from approximately 112 to 138 $m\mu$ seconds over a range of switching frequencies from 0.5 to 5.0 mc. Photographs
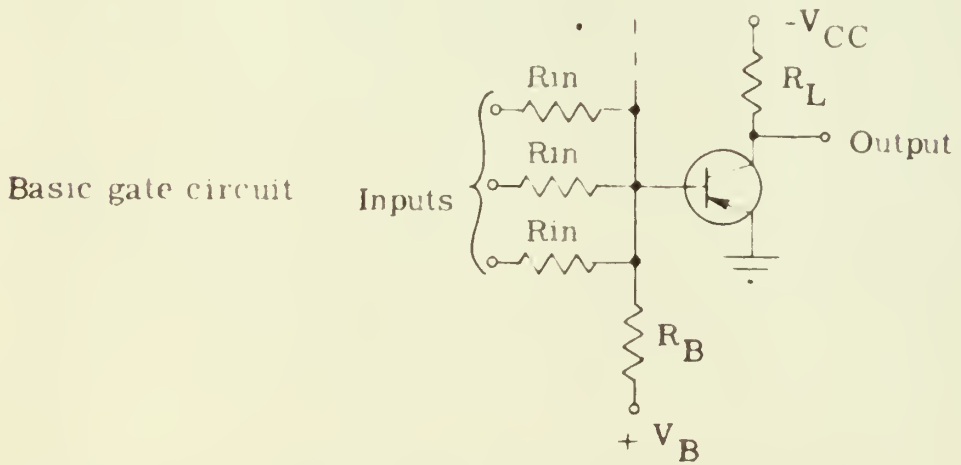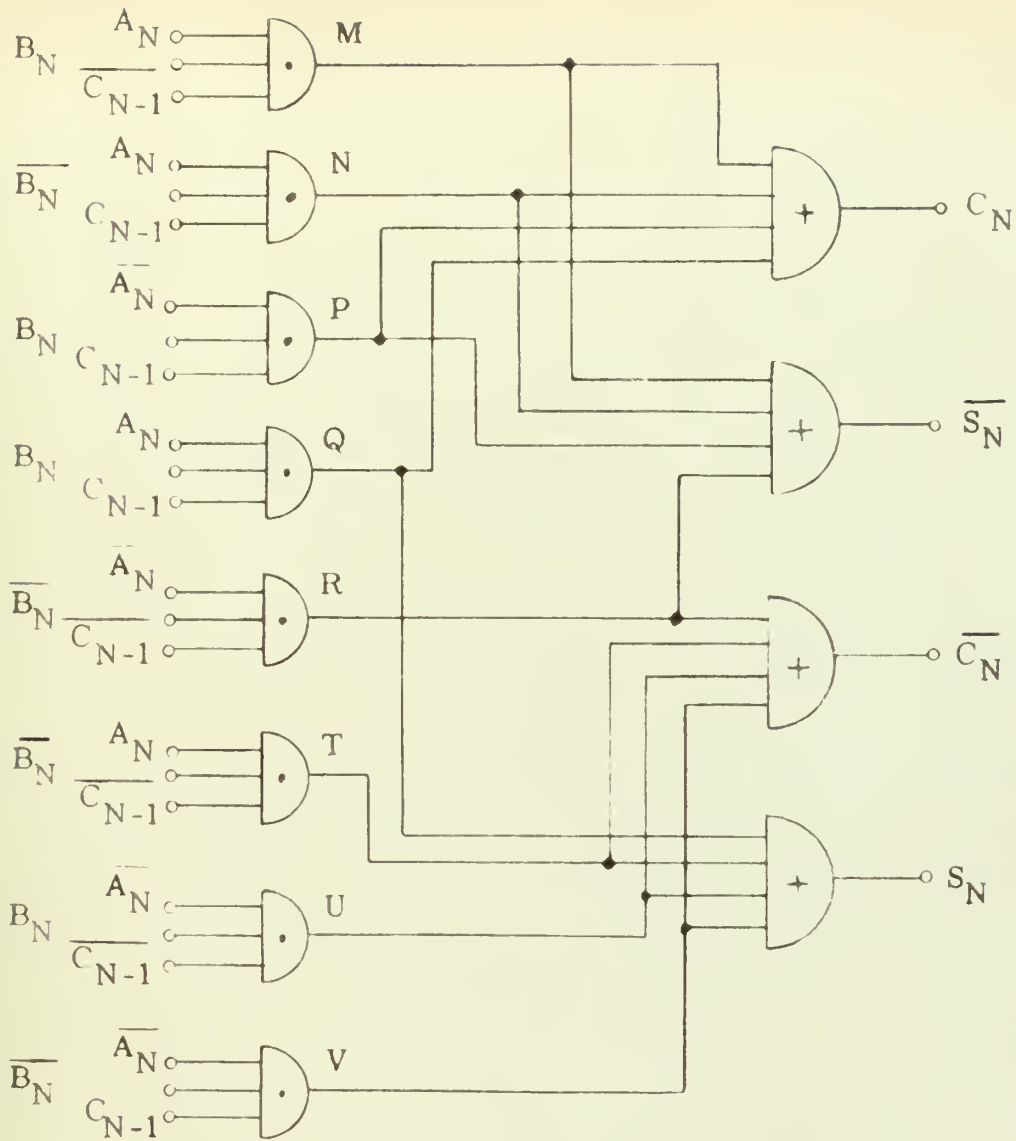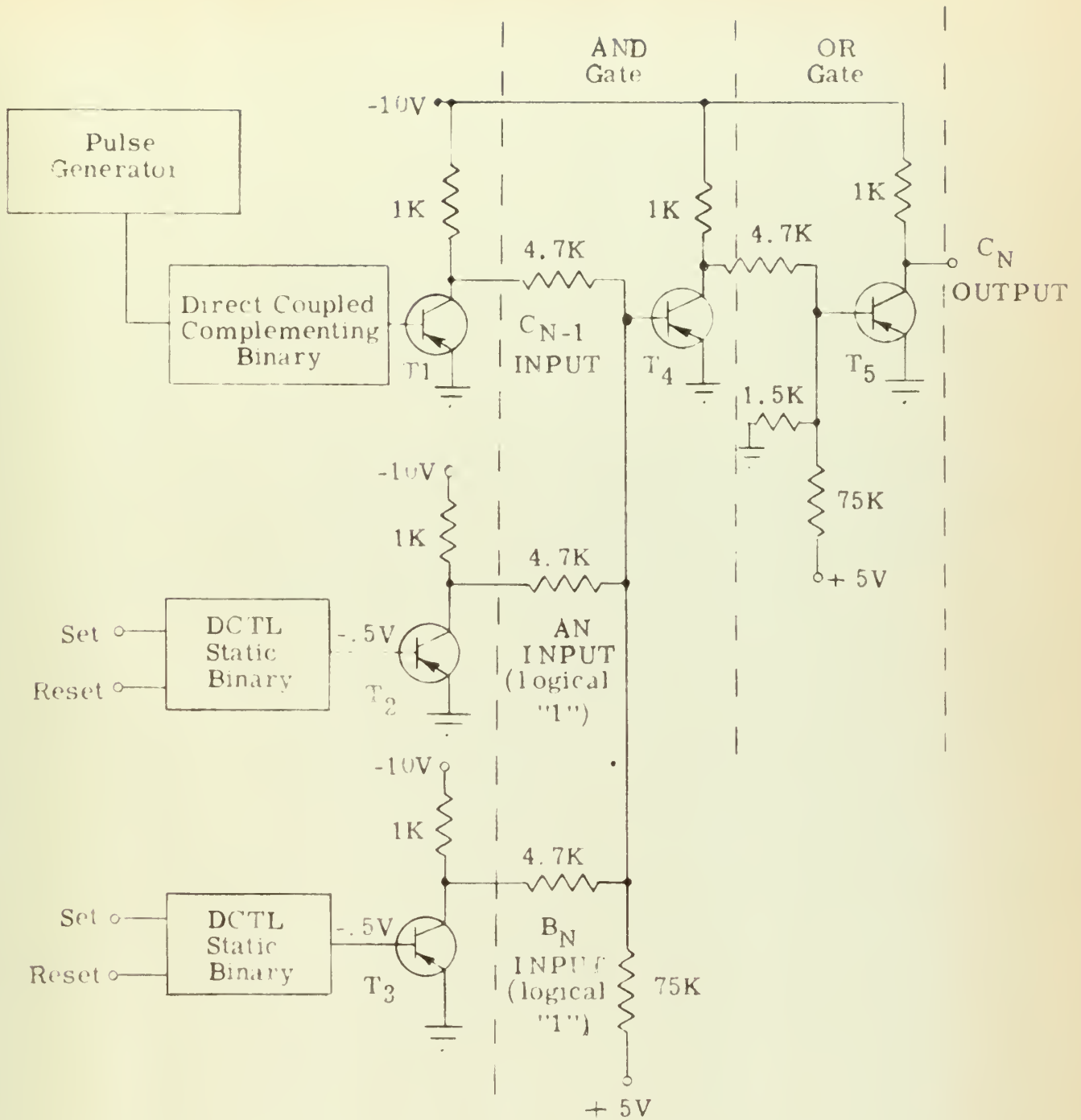
Figure 7.1. TRL Adder and the Basic Gate Circuit

All transistors: 2N501

Figure 7.2. TRL Adder Simulation Circuit

of typical input and output waveforms are shown in Figure 7. 5.

The TRL adder of Figure 7. 1 requires eight basic gate circuits employed as AND gates and four as OR gates, using a total of 12 transistors and 52 resistors. The power necessary to operate this configuration is approximately 945 milliwatts. Because the transistors in this study were operated only in the saturated and cutoff conditions, less stringent requirements in resistor value tolerance and supply voltage variation were possible. In this design satisfactory operation was obtained with resistors having 10% tolerance and supply voltage variation of approximately 15%. As the number of input and output channels to the gate circuit is increased, however, tolerances would have to be tightened.

Inspection of Figure 7. 1 shows that the TRL circuits require a greater number of components than a direct coupled system and approximately the same quantity as used in the diode configuration. It should be noted, however, that resistors have been utilized for the functions performed by transistors and diodes in the other systems.
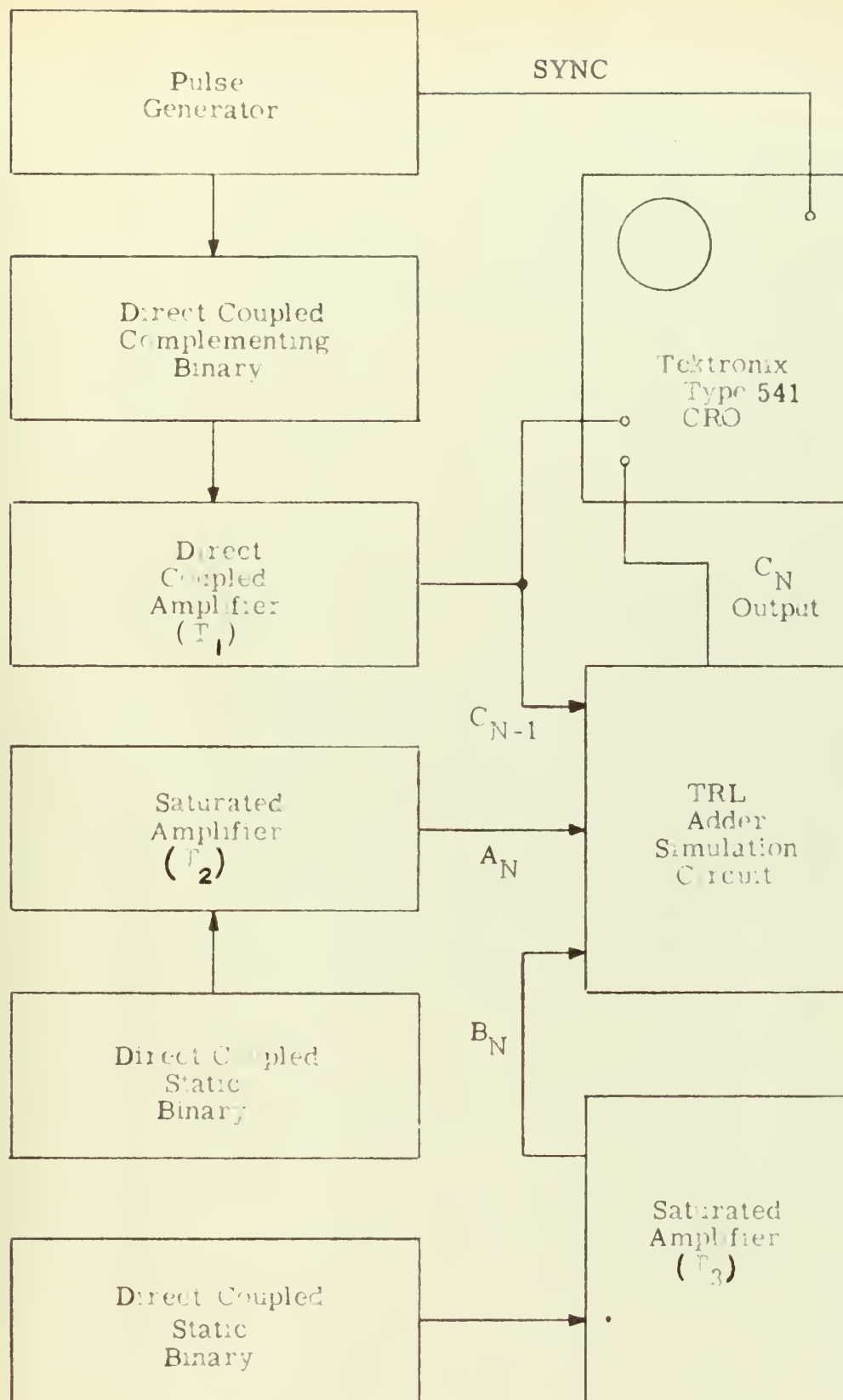
Figure 7.3. Measurement of Carry Propagation Time in the TRL System

38
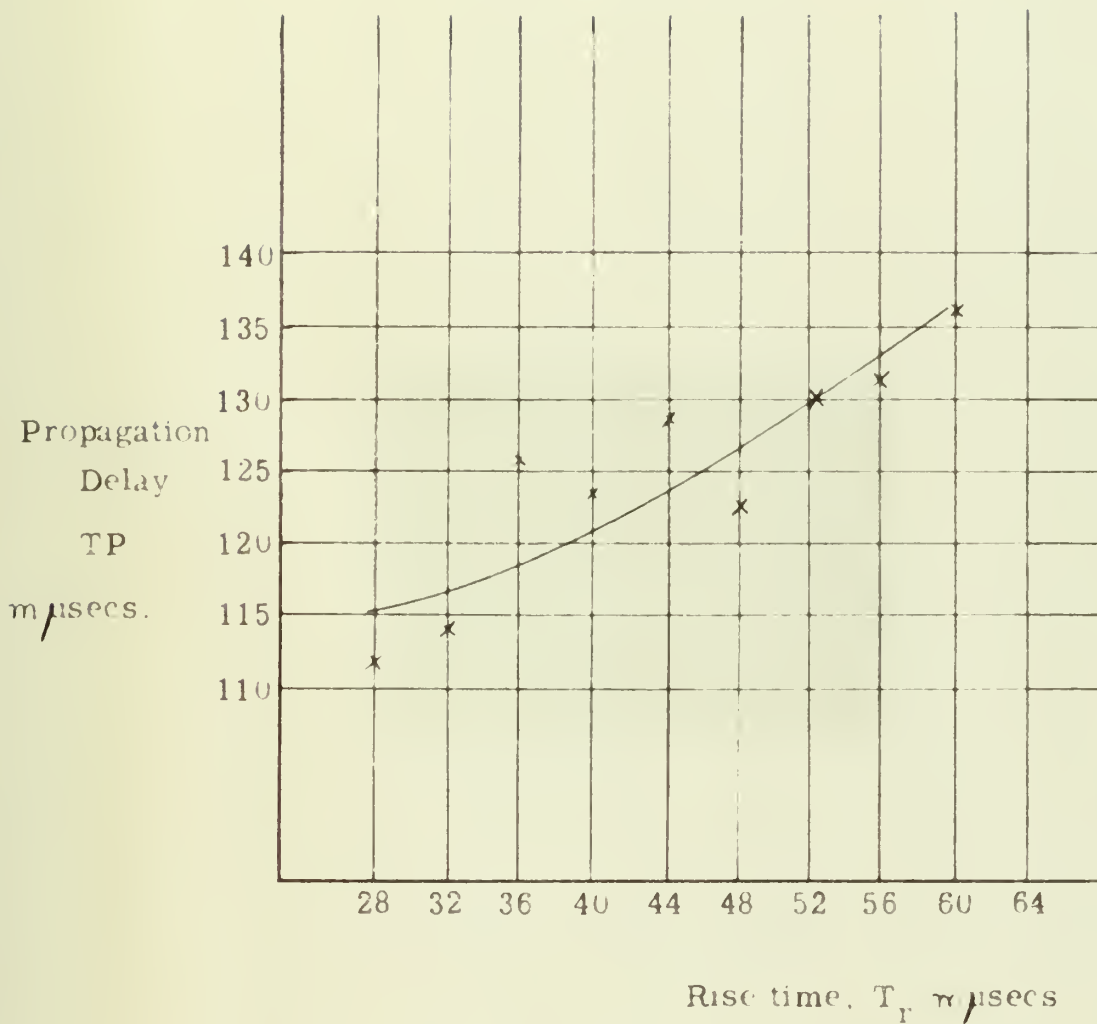
Figure 7.4. Propagation Delay Time vs Rise Time for the TRL System
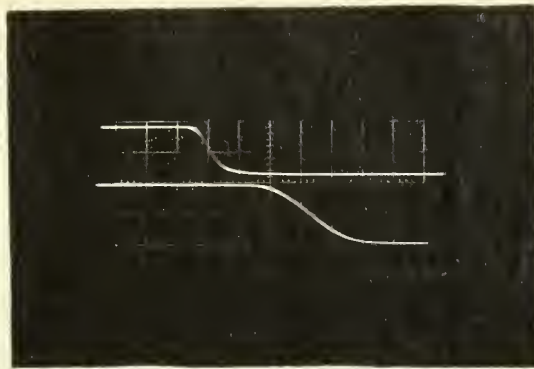
Upper: C_{N-1} input
Lower: C_N output
Horiz: 0.04 secs/div
Vert :   5.0 volts/div
T_p 126 musecs
T_r 36 musecs
f_{sw} 0.5 mc
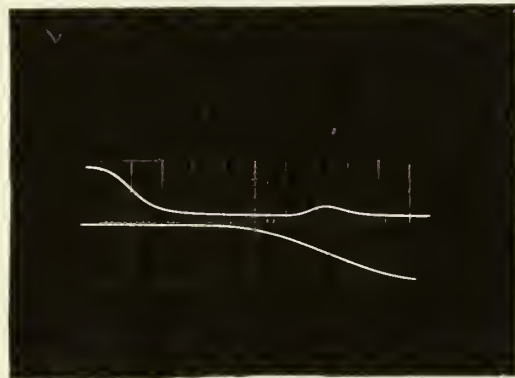
Upper: C_{N-1} input
Lower: C_N output
Horiz: 0.02 usecs/div
Vert :   5.0 volts/div
T_p 126 musecs
T_r 36 musecs
f_{sw} 2 mc

Figure 7.5 Photographs of input and output waveforms of the TRL
circuit at switching frequencies indicated

40

8. Conclusions

The study of high speed digital circuits using recent diffused base and drift transistors, as well as very fast switching diodes, showed that the best propagation time was obtained with the DCTL configuration. The average T_p for this type of circuitry was 17.5 mμ seconds over a range of 26 to 48 mμ seconds of T_r; f_{SW} was varied from 0.5 mc to 5.0 mc. The diode design was found to be slightly slower, i.e., required a greater T_p, and the TRL system extremely slow by comparison with the other two. If we interpret these data in terms of a ten-bit parallel adder, the intended application, comparison of the three systems is made in Table II.

System	Average time to add two 10-bit nos. (mμ secs.)	No. of Transistors	No. of Resistors	No. of Diodes	Power (mw)
DCTL	175	13	4	0	66
Diode*	330	4	26	28	204
TRL	1240	12	52	0	945

* Includes current amplifiers

Table II Comparison of the DCTL, Diode and TRL systems in a 10-bit parallel adder

In packaging the circuits the DCTL configuration was effected in approximately one-third the volume required by the diode and TRL designs. The power drain for the DCTL system was 66 mw, considerably less than the others and requiring only one value of supply voltage. The diode circuits operated at 204 mw and the TRL at 945 mw, both systems using two values of supply and bias voltage.

The study showed that DCTL circuitry is preferable in applications where high speed operation is necessary and where size and power consumption are critical. DCTL will be less attractive than the diode system from an economic standpoint and, in general, this will hold true for TRL also.

The use of drift and diffused base transistors in pulse circuitry was found to be particularly effective, the blocking oscillator and pulse forming stages demonstrating the high prf and circuit simplicity obtainable.

In view of the tremendous research and development efforts presently under way, future improvements in high speed semiconductor devices are certain and the design of faster and more compact circuitry employing these components will continue to challenge the computer engineer.

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8. Q. W. Simkins, Transistor Resistor Logic Circuit Analysis, Transistor & Solid-State Circuits Conference, February 20, 1958.

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TRANSISTOR CHARACTERISTICS

TRANSISTOR AND TYPE ( )	ABSOLUTE MAXIMUM RATINGS					TYPICAL RATINGS			SATURATION (TYPICAL)	
	V_{CE} (V)	I_C (ma)	V_{CB} (V)	P_d (mw)	T_j (oC)	$f_{\alpha co}$ (mc)	*I_{CO} (μa)	Max. $f_{osc.}$ (mc)	V_{BE} (V)	V_{CE} (V)
2N501 (DB)	-12	50	-15	25	85	200	1.0	350	-.37	-.05
2N384 (DR)	-30	10	-30	120	85	100	16	250	-.35	-.05
2N623 (DB)	-15	20	-30	40	65	90	10	200	-.38	-1.0

Transitron S570G Diode Specifications:

Maximum forward voltage at 10ma.......... 1.0V

Maximum inverse current at -6V......... 30.0 μa

Maximum inverse voltage at 100 μ amps.... 8.0V

Recovery time (max.) .... .002 μ sec.

Maximum continuous forward current...... 20.0 ma

DB - Diffused Base

DR - Drift

SB - Surface Barrier

* - Approximate value

APPENDIX II
LOGICAL EQUATIONS FOR THE BINARY ADDER

The Boolean expressions for the binary adder outputs as a function of its inputs are shown below with combination of terms for simplification of circuit design.

$$C_N = A_N B_N \overline{C_{N-1}} + A_N \overline{B_N} C_{N-1} + \overline{A_N} B_N C_{N-1} + A_N B_N C_{N-1}$$

$$= A_N B_N + \left[(A_N \overline{B_N} + \overline{A_N} B_N) \cdot C_{N-1} \right]$$

$$= A_N B_N + \left(S_N' \cdot C_{N-1} \right)$$

$$\overline{C_N} = \overline{A_N} \overline{B_N} C_{N-1} + A_N \overline{B_N} \overline{C_{N-1}} + \overline{A_N} B_N \overline{C_{N-1}} + \overline{A_N} \overline{B_N} C_{N-1}$$

$$= \overline{A_N} \overline{B_N} + \left[(\overline{A_N} B_N + A_N \overline{B_N}) \cdot \overline{C_{N-1}} \right]$$

$$= \overline{A_N} \overline{B_N} + \left(S_N' \cdot \overline{C_{N-1}} \right)$$

$$S_N = A_N \overline{B_N} \overline{C_{N-1}} + \overline{A_N} B_N \overline{C_{N-1}} + \overline{A_N} \overline{B_N} C_{N-1} + A_N B_N C_{N-1}$$

$$= \left[(A_N B_N + \overline{A_N} \overline{B_N}) \cdot C_{N-1} \right] + (A_N \overline{B_N} + \overline{A_N} B_N) \cdot \overline{C_{N-1}}$$

$$= \left(\overline{S_N'} \cdot C_{N-1} \right) + \left(S_N' \cdot \overline{C_{N-1}} \right)$$

$$\overline{S_N} = \overline{A_N} \overline{B_N} \overline{C_{N-1}} + A_N B_N \overline{C_{N-1}} + A_N \overline{B_N} C_{N-1} + \overline{A_N} B_N C_{N-1}$$

$$= \left[(\overline{A_N} \overline{B_N} + A_N B_N) \cdot \overline{C_{N-1}} \right] + \left[(A_N \overline{B_N} + \overline{A_N} B_N) \cdot C_{N-1} \right]$$

$$= \left(\overline{S_N'} \cdot \overline{C_{N-1}} \right) + \left(S_N' \cdot C_{N-1} \right)$$